

02/06/2007 10/710826 Doty

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(FILE 'HOME' ENTERED AT 12:02:14 ON 06 FEB 2007)

FILE 'REGISTRY' ENTERED AT 12:02:38 ON 06 FEB 2007

L1 758 SEA ABB=ON PLU=ON GE.SI/MF  
L2 46 SEA ABB=ON PLU=ON GE SI/ELF  
L3 2931 SEA ABB=ON PLU=ON (SI AND GE)/MAC

FILE 'CAPLUS' ENTERED AT 12:05:59 ON 06 FEB 2007

L4 18315 SEA ABB=ON PLU=ON L1 OR L2  
L5 402 SEA ABB=ON PLU=ON L4 (L) INSULATOR  
L6 19556 SEA ABB=ON PLU=ON L3  
L7 402 SEA ABB=ON PLU=ON L5 AND L6  
L8 60124 SEA ABB=ON PLU=ON SUPERLATTIC? OR SUPER(W)LATTIC? OR  
(DIGITAL? OR MULTILAYER? OR MULTI?(2W)LAYER? OR ?STACK?) (3W)ALL  
O? OR MULITLAYER? OR MULTI?(2W)LAYER?  
L9 1309 SEA ABB=ON PLU=ON L6 AND L8  
L10 13 SEA ABB=ON PLU=ON L9 AND L7  
D IBIB ABS HITSTR HITIND 1-13

FILE 'STNGUIDE' ENTERED AT 12:20:08 ON 06 FEB 2007

FILE 'CAPLUS' ENTERED AT 12:24:19 ON 06 FEB 2007

L11 46897 SEA ABB=ON PLU=ON SIGE OR (SI OR SILICON) (2A) (GERMANIUM OR  
GE)  
L12 256 SEA ABB=ON PLU=ON SGOI OR (SIGE OR SILICON-GERMANIUM) (2W) INSU  
LAT?  
L13 50219 SEA ABB=ON PLU=ON L1 OR L2 OR L3 OR L11  
L14 12 SEA ABB=ON PLU=ON L13 AND L8 AND L12  
L15 8 SEA ABB=ON PLU=ON L14 NOT L10  
D IBIB ABS HITSTR HITIND 1-8

FILE 'STNGUIDE' ENTERED AT 12:33:39 ON 06 FEB 2007

FILE 'CAPLUS' ENTERED AT 12:37:57 ON 06 FEB 2007

L16 12 SEA ABB=ON PLU=ON L12 AND L8  
L17 0 SEA ABB=ON PLU=ON L16 NOT (L10 OR L15)  
L18 2221 SEA ABB=ON PLU=ON L13 AND L8

FILE 'CAPLUS' ENTERED AT 12:58:14 ON 06 FEB 2007

L19 12 SEA ABB=ON PLU=ON L18 AND L12  
L20 0 SEA ABB=ON PLU=ON L19 NOT (L10 OR L15)  
L21 13 SEA ABB=ON PLU=ON L5 AND L18  
L22 0 SEA ABB=ON PLU=ON L21 NOT (L10 OR L15)  
L23 5 SEA ABB=ON PLU=ON L18 AND (DIGITAL ALLOY)  
L24 5 SEA ABB=ON PLU=ON L23 NOT (L10 OR L15)  
D IBIB ABS HITSTR HITIND 1-5

FILE 'WPIX' ENTERED AT 13:04:11 ON 06 FEB 2007

L25 50922 SEA ABB=ON PLU=ON SUPERLATTIC? OR SUPER(W)LATTIC? OR  
(DIGITAL? OR MULTILAYER? OR MULTI?(2W)LAYER? OR ?STACK?) (3W)ALL  
O? OR MULITLAYER? OR MULTI?(2W)LAYER?  
L26 15186 SEA ABB=ON PLU=ON SIGE OR (SI OR SILICON) (2A) (GERMANIUM OR  
GE)  
L27 163 SEA ABB=ON PLU=ON SGOI OR (SIGE OR SILICON-GERMANIUM) (2W) INSU

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LAT?

L28 6 SEA ABB=ON PLU=ON L25 AND L27  
D IFULL 1-6

FILE 'WPIX' ENTERED AT 13:14:42 ON 06 FEB 2007

L29 8 SEA ABB=ON PLU=ON DIGITAL ALLOY  
L30 7 SEA ABB=ON PLU=ON L29 NOT L28  
D IALL 1-7

FILE 'JAPIO, KOREAPAT' ENTERED AT 13:34:43 ON 06 FEB 2007

L31 22018 SEA ABB=ON PLU=ON L8  
L32 4750 SEA ABB=ON PLU=ON L11  
L33 23 SEA ABB=ON PLU=ON L12 OR SI-GEOI  
L34 0 SEA ABB=ON PLU=ON L31 AND L33  
L35 20 SEA ABB=ON PLU=ON L33 AND L32  
L36 20 DUP REM L35 (0 DUPLICATES REMOVED)  
D IALL 1-20

FILE 'INSPEC' ENTERED AT 13:58:51 ON 06 FEB 2007

L37 0 SEA ABB=ON PLU=ON (SI EL(S)GE EL(S)SIGE SS)/CHI  
L38 38 SEA ABB=ON PLU=ON (SI EL(S)GE EL(S)SIGE INT)/CHI  
L39 13940 SEA ABB=ON PLU=ON (SI BIN(S)GE BIN)/CHI  
L40 2929 SEA ABB=ON PLU=ON (SI EL(S)GE EL)/CHI  
L41 38 SEA ABB=ON PLU=ON (SI EL(S)GE EL(S)SIGE BIN)/CHI  
L42 16055 SEA ABB=ON PLU=ON L39 OR L40  
L43 56099 SEA ABB=ON PLU=ON SUPERLATTIC? OR SUPER(W)LATTIC? OR  
(DIGITAL? OR MULTILAYER? OR MULTI?(2W)LAYER? OR ?STACK?) (3W)ALL  
O? OR MULITLAYER? OR MULTI?(2W)LAYER?  
L44 31001 SEA ABB=ON PLU=ON SIGE OR (SI OR SILICON) (2A) (GERMANIUM OR  
GE)  
L45 204 SEA ABB=ON PLU=ON L12 OR SI-GEOI  
L46 31373 SEA ABB=ON PLU=ON L42 OR L44  
L47 1991 SEA ABB=ON PLU=ON L43 AND L46  
L48 2 SEA ABB=ON PLU=ON L45 AND L47  
D IALL 1-2  
L49 122 SEA ABB=ON PLU=ON DIGITAL ALLOY  
L50 0 SEA ABB=ON PLU=ON L41 AND L49  
L51 1 SEA ABB=ON PLU=ON L47 AND L49  
D IALL  
L52 3 SEA ABB=ON PLU=ON L41 AND L43  
L53 3 SEA ABB=ON PLU=ON L52 NOT (L48 OR L51)  
D IALL 1-3  
L54 198 SEA ABB=ON PLU=ON L45 AND L46  
L55 192257 SEA ABB=ON PLU=ON MOSFET OR MOS OR FET OR MOS OR PMOS OR  
NMOS? OR CMOS? OR METAL OXIDE SEMICONDU? OR FIELD EFFECT  
L56 106 SEA ABB=ON PLU=ON L54 AND L55  
L57 103 SEA ABB=ON PLU=ON L56 AND INSULAT?  
L58 66 SEA ABB=ON PLU=ON L57 AND SUBSTRAT?  
D TI 1-66  
D IALL 1-66  
L59 11 SEA ABB=ON PLU=ON L58 AND PY>2005  
L60 55 SEA ABB=ON PLU=ON L58 NOT L59  
D IALL 1-55

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L10 ANSWER 4 OF 13 CAPLUS COPYRIGHT 2007 ACS on STN

ACCESSION NUMBER: 2005:99736 CAPLUS

DOCUMENT NUMBER: 142:188807

TITLE: Deposition of SiGe on silicon-on-insulator structures and bulk substrates

INVENTOR(S): Bauer, Matthias

PATENT ASSIGNEE(S): Asm America, Inc., USA

SOURCE: PCT Int. Appl., 27 pp.

CODEN: PIXXD2

DOCUMENT TYPE: Patent

LANGUAGE: English

FAMILY ACC. NUM. COUNT: 1

PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
WO 2005010946	A2	20050203	WO 2004-US23505	20040721
WO 2005010946	A3	20060908		
EP 1647046	A2	20060419	EP 2004-757193	20040721
US 2005054175	A1	20050310	US 2004-897985	20040723
PRIORITY APPLN. INFO.:			US 2003-489691P	P 20030723
			WO 2004-US23505	W 20040721

AB The invention relates to a process for making a SiGe-on-insulator structure strain-relaxed SiGe layer on a silicon wafer while minimizing defects. Amorphous SiGe layers are deposited by CVD from trisilane and GeH<sub>4</sub>. The amorphous SiGe layers are recrystd. over silicon by melt or solid phase epitaxy (SPE) processes. The melt processes preferably also cause diffusion of germanium to dilute the overall germanium content and essentially consume the silicon overlying the insulator. The SPE process can be conducted with or without diffusion of germanium into the underlying silicon, and so is applicable to SOI as well as conventional semiconductor substrates.

IT 11148-21-3

RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)  
(CVD of SiGe on silicon-on-insulator structure and bulk substrate)

RN 11148-21-3 CAPLUS

CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component Component  
Registry Number

=====+=====

Ge 7440-56-4

Si 7440-21-3

IC ICM H01L

CC 76-3 (Electric Phenomena)

ST CVD SPE SOI diffusion silicon germanium **superlattice**

IT Diffusion

SOI devices

Solid phase epitaxy

**Superlattices**

(CVD of SiGe on silicon-on-insulator structure and bulk substrate)

IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes

11148-21-3

EIC 2800 MARY S. MIMS 272-5928

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L10 ANSWER 5 OF 13 CAPLUS COPYRIGHT 2007 ACS on STN

ACCESSION NUMBER: 2005:46483 CAPLUS

DOCUMENT NUMBER: 143:336802

TITLE: Fabrication of nanoscale strained silicon grown on relaxed SiGe on insulator for beyond submicron CMOSFET

AUTHOR(S): Park, Jea-Gun

CORPORATE SOURCE: Nano-SOI Process Laboratory, Hanyang University, S. Korea

SOURCE: Chaeryo Madang (2004), 17(5), 16-22

CODEN: CMADFK

PUBLISHER: Korean Institute of Metals and Materials

DOCUMENT TYPE: Journal; General Review

LANGUAGE: Korean

AB A review on the submicron CMOS process for the fabrication of strained silicon grown on relaxed SiGe on insulator for MOSFET integrated circuits.

IT 11148-21-3

RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)

(submicron CMOS process for fabrication of strained silicon grown on relaxed SiGe on insulator for MOSFET integrated circuit)

RN 11148-21-3 CAPLUS

CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component Component  
Registry Number

=====+=====

Ge 7440-56-4

Si 7440-21-3

CC 76-0 (Electric Phenomena)

IT Integrated circuits

MOSFET (transistors)

SOI devices

**Superlattice devices**

(submicron CMOS process for fabrication of strained silicon grown on relaxed SiGe on insulator for MOSFET integrated circuit)

IT 7440-21-3, Silicon, processes 11148-21-3

RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)

(submicron CMOS process for fabrication of strained silicon grown on relaxed SiGe on insulator for MOSFET integrated circuit)

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L15 ANSWER 8 OF 8 CAPLUS COPYRIGHT 2007 ACS on STN

ACCESSION NUMBER: 2001:389032 CAPLUS

DOCUMENT NUMBER: 135:13032

TITLE: Fabrication of semiconductor devices involving  
formation of thin **SiGe** layer on  
**insulating** layer and semiconductor devices  
having strained Si layer thereon

INVENTOR(S): Sugiyama, Naoharu; Mizuno, Tomohisa; Takagi, Shinichi;  
Kurobe, Atsushi

PATENT ASSIGNEE(S): Toshiba Corp., Japan

SOURCE: Jpn. Kokai Tokkyo Koho, 10 pp.

CODEN: JKXXAF

DOCUMENT TYPE: Patent

LANGUAGE: Japanese

FAMILY ACC. NUM. COUNT: 1

PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001148473	A	20010529	JP 2000-270251	20000906
US 6326667	B1	20011204	US 2000-658191	20000908
			JP 1999-255154	A 19990909

PRIORITY APPLN. INFO.:

AB The process involves forming a strained **SiGe** layer on a substrate, injecting O ions, heating to form an oxide layer in the **SiGe** layer and to relax the lattice of the strained **SiGe** layer upon the oxide layer, and growing a strained Si layer on the lattice-relaxed **SiGe** layer. Preferably, a Si capping layer is formed on the strained **SiGe** layer to protect it in the heating process. On the lattice-relaxed **SiGe** may be formed a **SiGe** layer whereupon the strained Si layer will be formed. Before forming the strained Si layer, the surface of the lattice-relaxed **SiGe** layer may be etched. The surface of the lattice-relaxed **SiGe** layer may be treated with HF to form a H-terminated surface whereupon the strained Si layer will be formed. The H on the surface of the lattice-relaxed **SiGe** layer are preferably removed. After the oxidation process to form the oxide layer on the lattice-relaxed **SiGe** layer, the oxide layer may be removed by heating in vacuo, then the strained Si layer will be formed thereon. Preferably, on the substrate is formed a **SiGe** buffer layer whereupon the strained **SiGe** layer will be formed. Preferably, the substrate is Si or a SOI (silicon on insulator) type. The resulting semiconductor device comprises 1st **SiGe** layer on a substrate, an oxide layer on the 1st **SiGe** layer,  $\leq 200$ -nm thick 2nd **SiGe** layer lattice-relaxed and formed on the oxide layer, and a strained Si layer on the 2nd **SiGe** layer.

IT 59027-94-0, Germanium 0-20, silicon 80-100  
(atomic)

RL: DEV (Device component use); USES (Uses)

(buffer; manufacture of semiconductor devices with insulating layer/thin **SiGe**/strained Si layer structure)

RN 59027-94-0 CAPLUS

CN Silicon alloy, base, Si 61-100, Ge 0-39 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Si	61 - 100	7440-21-3
Ge	0 - 39	7440-56-4

EIC 2800 MARY S. MIMS 272-5928

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IT 37380-03-3  
RL: DEV (Device component use); USES (Uses)  
(lattice-relaxed; manufacture of semiconductor devices with insulating  
layer/thin SiGe/strained Si layer structure)  
RN 37380-03-3 CAPLUS  
CN Silicon alloy, base, Si 61,Ge 39 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Si	61	7440-21-3
Ge	39	7440-56-4

IT 12623-04-0 37232-85-2  
RL: NUU (Other use, unclassified); USES (Uses)  
(lattice-relaxed; manufacture of semiconductor devices with insulating  
layer/thin SiGe/strained Si layer structure)  
RN 12623-04-0 CAPLUS  
CN Germanium alloy, base, Ge 53,Si 47 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Ge	53	7440-56-4
Si	47	7440-21-3

RN 37232-85-2 CAPLUS  
CN Silicon alloy, base, Si 69,Ge 31 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Si	69	7440-21-3
Ge	31	7440-56-4

IC ICM H01L027-12  
ICS H01L021-205; H01L029-786  
CC 76-3 (Electric Phenomena)  
ST semiconductor device fabrication strained silicon layer; strained layer  
superlattice semiconductor device fabrication; silicon  
germanium underlayer formation semiconductor device; substrate SOI  
semiconductor device strained silicon  
IT MOSFET (transistors)  
Semiconductor device fabrication  
Semiconductor devices  
(manufacture of semiconductor devices with insulating layer/thin  
SiGe/strained Si layer structure)  
IT SOI devices  
(manufacture of semiconductor devices with insulating layer/thin  
SiGe/strained Si layer structure on SOI substrates)  
IT 59027-94-0, Germanium 0-20, silicon 80-100  
(atomic)  
RL: DEV (Device component use); USES (Uses)  
(buffer; manufacture of semiconductor devices with insulating layer/thin  
SiGe/strained Si layer structure)  
IT 116551-27-0, Silicon oxide (SiOx)  
RL: DEV (Device component use); USES (Uses)  
(buried oxide layer; manufacture of semiconductor devices with insulating

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layer/thin SiGe/strained Si layer structure)  
IT 37380-03-3  
RL: DEV (Device component use); USES (Uses)  
(lattice-relaxed; manufacture of semiconductor devices with insulating  
layer/thin SiGe/strained Si layer structure)  
IT 12623-04-0 37232-85-2  
RL: NUU (Other use, unclassified); USES (Uses)  
(lattice-relaxed; manufacture of semiconductor devices with insulating  
layer/thin SiGe/strained Si layer structure)  
IT 7440-21-3, Silicon, uses  
RL: DEV (Device component use); USES (Uses)  
(strained; manufacture of semiconductor devices with insulating layer/thin  
SiGe/strained Si layer structure)



L15 ANSWER 7 OF 8 CAPLUS COPYRIGHT 2007 ACS on STN

ACCESSION NUMBER: 2003:538866 CAPLUS

DOCUMENT NUMBER: 139:253185

TITLE: Oxygen profile engineering in **silicon** by **germanium** addition and high-temperature annealing

AUTHOR(S): An, Zhenghua; Chu, Paul K.; Zhang, Miao; Men, Chuanling; Lin, Chenglu

CORPORATE SOURCE: Department of Physics and Material Science, City University of Hong Kong, Kowloon, Hong Kong, Peop. Rep. China

SOURCE: Applied Physics Letters (2003), 83(2), 305-307

CODEN: APPLAB; ISSN: 0003-6951

PUBLISHER: American Institute of Physics

DOCUMENT TYPE: Journal

LANGUAGE: English

AB The formation of multilayer structures in oxygen-implanted silicon by the introduction of germanium is reported. The oxygen distribution can be split under carefully controlled annealing conditions. The typical annealing process consists of 1st raising the furnace temperature from 600 to 1200° within 30 min and then holding the temperature at 1200° for 2 h. The faster crystallization rate of amorphous **silicon** **germanium** (SiGe) and germanium rejection from the oxide contribute to the final multilayer structure. The findings suggest that oxygen profile engineering is possible and single-energy ion implantation can be used to fabricate multilayer structures containing **multiple** buried oxide **layers**. The authors' results suggest that, in **SiGe-on-insulator** fabrication, the annealing step at a moderate temperature or a slow temperature ramp-up rate during the high-temperature annealing step is much more critical than in conventional silicon-on-insulator fabrication.

IT 11148-21-3P

RL: DEV (Device component use); PNU (Preparation, unclassified); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses) (oxygen profile engineering in **silicon** by **germanium** addition and high-temperature annealing in multilayer structure formation in integrated devices)

RN 11148-21-3 CAPLUS

CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component Component  
Registry Number

=====+=====

Ge 7440-56-4

Si 7440-21-3

CC 76-3 (Electric Phenomena)

IT Ion implantation  
(buried oxide; oxygen profile engineering in **silicon** by **germanium** addition and high-temperature annealing in multilayer structure formation in integrated devices)

IT Distribution function  
(depth; oxygen profile engineering in **silicon** by **germanium** addition and high-temperature annealing in multilayer structure formation in integrated devices)

IT Annealing  
(high-temperature; oxygen profile engineering in **silicon** by



germanium addition and high-temperature annealing in multilayer structure formation in integrated devices)

IT Crystallization  
(oxygen profile engineering in silicon by germanium addition and high-temperature annealing in multilayer structure formation in integrated devices)

IT Oxides (inorganic), uses  
RL: DEV (Device component use); PNU (Preparation, unclassified); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)  
(oxygen profile engineering in silicon by germanium addition and high-temperature annealing in multilayer structure formation in integrated devices)

IT Semiconductor device fabrication  
(oxygen profile engineering; oxygen profile engineering in silicon by germanium addition and high-temperature annealing in multilayer structure formation in integrated devices)

IT 7440-21-3P, Silicon, uses 7440-56-4P; Germanium, uses 11148-21-3P 113443-18-8P, Simox  
RL: DEV (Device component use); PNU (Preparation, unclassified); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)  
(oxygen profile engineering in silicon by germanium addition and high-temperature annealing in multilayer structure formation in integrated devices)

IT 7782-44-7, Oxygen, properties  
RL: PRP (Properties); RCT (Reactant); RACT (Reactant or reagent)  
(oxygen profile engineering in silicon by germanium addition and high-temperature annealing in multilayer structure formation in integrated devices)

REFERENCE COUNT: 21 THERE ARE 21 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

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L24 ANSWER 4 OF 5 CAPLUS COPYRIGHT 2007 ACS on STN

ACCESSION NUMBER: 2004:3188 CAPLUS

DOCUMENT NUMBER: 140:69017

TITLE: Design and fabrication of a strained silicon p-type MOSFET having improved hole mobility enhancement

INVENTOR(S): Lee, Minjoo L.; Fitzgerald, Eugene

PATENT ASSIGNEE(S): Massachusetts Institute of Technology, USA

SOURCE: PCT Int. Appl., 16 pp.

CODEN: PIXXD2

DOCUMENT TYPE: Patent

LANGUAGE: English

FAMILY ACC. NUM. COUNT: 1

PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
WO 2004001811	A2	20031231	WO 2003-US20129	20030625
WO 2004001811	A3	20040226		

AU 2003247712	A1	20040106	AU 2003-247712	20030625
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US 2004053470	A1	20040318	US 2003-603712	20030625
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PRIORITY APPLN. INFO.: US 2002-391452P P 20020625

WO 2003-US20129 W 20030625

AB The invention relates to the design and fabrication of a strained silicon p-type MOSFET having improved hole mobility enhancement, where the structure contains alternating layers of relaxed SiGe and  $\epsilon$ -Si. The fabrication consists of the steps of (i) providing a substrate; (ii) forming a relaxed SiGe layer on the substrate having a Ge content between 0.51 and 0.8; and (iii) forming on the relaxed SiGe layer a digital alloy structure consisting of alternating layers of  $\epsilon$ -Si and SiGe having a Ge content between 0.51 and 1, such that the mobility enhancement of the device is constant

IT 639001-46-0 639001-47-1

RL: DEV (Device component use); USES (Uses)

(design and fabrication of strained silicon p-type MOSFET having improved hole mobility enhancement)

RN 639001-46-0 CAPLUS

CN Germanium alloy, base, Ge 73-91, Si 8.8-27 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Ge	73 - 91	7440-56-4
Si	8.8 - 27	7440-21-3

RN 639001-47-1 CAPLUS

CN Germanium alloy, base, Ge 73-100, Si 0-27 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Ge	73 - 100	7440-56-4
Si	0 - 27	7440-21-3

IC ICM H01L

CC 76-3 (Electric Phenomena)

Section cross-reference(s): 75

EIC 2800 MARY S. MIMS 272-5928

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IT 639001-46-0 639001-47-1

RL: DEV (Device component use); USES (Uses)

(design and fabrication of strained silicon p-type MOSFET having improved hole mobility enhancement)

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L28 ANSWER 4 OF 6 WPIX COPYRIGHT 2007 THE THOMSON CORP on STN  
ACCESSION NUMBER: 2003-900175 [82] WPIX  
DOC. NO. CPI: C2003-256025 [82]  
DOC. NO. NON-CPI: N2003-718576 [82]  
TITLE: Fabrication of relaxed **silicon**  
**germanium-on-insulator** substrate by  
implanting oxygen ions into **multi-layer**  
heterostructure comprising alternating layers of silicon  
and silicon-germanium, and annealing **multi-**  
**layer** heterostructure  
DERWENT CLASS: L03; U11  
INVENTOR: CHU J O; HUANG F; KOESTER S J; SADANA D K  
PATENT ASSIGNEE: (IBMC-C) INT BUSINESS MACHINES CORP  
COUNTRY COUNT: 1

PATENT INFORMATION:

PATENT NO	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 20030199126	A1	20031023	(200382)*	EN	10 [6]	H01L021-00
US 6743651	B2	20040601	(200436)	EN		H01L021-00

APPLICATION DETAILS:

PATENT NO	KIND	APPLICATION	DATE
US 20030199126	A1	US 2002-128794	20020423

PRIORITY APPLN. INFO: US 2002-128794 20020423

INT. PATENT CLASSIF.:

IPC RECLASSIF.: H01L0021-70 [I,C]; H01L0021-762 [I,A]

BASIC ABSTRACT:

US 20030199126 A1 UPAB: 20060121

NOVELTY - Fabrication of relaxed **silicon**  
**germanium-on-insulator** substrate includes implanting  
oxygen ions into a **multi-layer** heterostructure  
comprising alternating layers of silicon and silicon-germanium and having  
an uppermost layer of silicon-germanium, and annealing the **multi**  
**-layer** heterostructure containing implanted oxygen ions to form  
a buried oxide region within one of the silicon layers.

USE - For fabricating relaxed **SiGe-on-insulator**  
substrate.

ADVANTAGE - The inventive method produces high-quality relaxed  
**SiGe-on-insulator** substrate.

DESCRIPTION OF DRAWINGS - The figure is a pictorial view of a  
**multi-layer** heterostructure.

Si layers (20)

SiGe layers (22)

TECHNOLOGY FOCUS:

ELECTRONICS - Preferred Method: The silicon (Si) layers (20) are  
formed by chemical vapor deposition, plasma-enhanced chemical vapor  
deposition, or epitaxial growth. The silicon-germanium (SiGe) layers (22)  
are formed by low-pressure chemical vapor deposition, ultra-high vacuum  
chemical vapor deposition, molecular beam epitaxy, plasma-enhanced  
chemical vapor deposition, rapid thermal chemical vapor deposition, or  
low-energy plasma process. The implanting step is performed using a  
separation by ion implantation of oxygen (SIMOX) process, e.g. high-dose  
oxygen implantation utilizing an ion dose of at least  $4 \times 10^{17}/\text{cm}^2$ , or

low-dose oxygen ion implantation utilizing an ion dose of at most  $4 \times 10^{17}/\text{cm}^2$ . A Si capping layer is formed on uppermost SiGe layer either before or after step oxygen implantation is performed. Prior to oxygen, a patterned dielectric mask is formed on the heterostructure to form discrete and isolated buried oxide regions in heterostructure after, and a Si capping layer is formed on exposed surfaces of heterostructure not containing the patterned dielectric mask; or a Si capping layer is formed on the heterostructure and a patterned dielectric mask is formed on the Si capping layer. Annealing is performed at 1000-1375 degrees C for 1-100 hours in non-oxidizing or oxidizing ambient. Preferred Components: The **multi-layer** heterostructure comprises a Si base layer and a SiGe uppermost layer. The Si layers comprise undoped single crystal Si, doped single-crystal Si, and/or epitaxial Si. The SiGe layers are graded or ungraded. The SiGe layers are crystalline and relaxed. They comprise at least 1 (preferably 5-30 atomic%) germanium. The SiGe layers above the buried oxide layer maintain their initial Ge content. The Si capping layer comprises polycrystalline Si, epitaxial Si, amorphous Si, and/or undoped or doped single crystal Si. Preferred Dimensions: Each Si layer has a thickness of 1-1000 nm. Each SiGe layer has thickness of 1-1000 nm. The Si capping layer has a thickness of 1-50 nm. After annealing, the uppermost SiGe layer has a thickness of at most 1000 Angstrom. The buried oxide layers have a thickness of 30-200 nm. Preferred Properties: The SiGe layers have a defect density of at most  $1 \times 10^7$  defects/cm<sup>2</sup> and a measured relaxation value of 0-100%.

INORGANIC CHEMISTRY - Preferred Gas: The oxidizing ambient comprises at least one oxygen-containing gas optionally admixed with inert gas, chlorine-containing gas or liquid, or combination of inert gas and chlorine-containing gas or liquid. The oxygen-containing gas comprises oxygen, nitric oxide, nitrous oxide, ozone, or air.

FILE SEGMENT: CPI; EPI  
 MANUAL CODE: CPI: L04-C02B; L04-C12C  
 EPI: U11-C02B2; U11-C02J1C; U11-C02J2; U11-C08A6

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L28 ANSWER 5 OF 6 WPIX COPYRIGHT 2007 THE THOMSON CORP on STN  
ACCESSION NUMBER: 2002-405425 [43] WPIX  
DOC. NO. CPI: C2002-113892 [43]  
DOC. NO. NON-CPI: N2002-318286 [43]  
TITLE: Preparation of relaxed silicon  
germanium layer on insulator and  
silicon germanium/silicon heterostructure by smoothing  
relaxed layer surface and bonding top surface of relaxed  
layer on first substrate to second substrate  
DERWENT CLASS: L03; U11  
INVENTOR: CHU J O; DIMILIA D; DIMILIA D R; HUANG L  
PATENT ASSIGNEE: (IBMC-C) IBM CORP; (IBMC-C) IBM UK LTD; (IBMC-C) INT  
BUSINESS MACHINES CORP  
COUNTRY COUNT: 97

PATENT INFORMATION:

PATENT NO	KIND	DATE	WEEK	LA	PG	MAIN IPC
WO 2002033746	A1	20020425	(200243)*	EN	18 [6]	H01L021-762
AU 2001087881	A	20020429	(200255)	EN		
EP 1327263	A1	20030716	(200347)	EN		H01L021-762
TW 521395	A	20030221	(200364)	ZH		H01L021-8238
KR 2003051714	A	20030625	(200373)	KO		H01L021-20
JP 2004512683	W	20040422	(200428)	JA	29	H01L027-12
CN 1531751	A	20040922	(200503)	ZH		
US 6890835	B1	20050510	(200532)	EN		H01L021-30
US 20050104067	A1	20050519	(200534)	EN		H01L029-10

PRIORITY APPLN. INFO: US 2000-692606 20001019  
US 2004-948421 20040923

INT. PATENT CLASSIF.:

MAIN: H01L021-20; H01L021-8238; H01L027-12  
IPC RECLASSIF.: H01L0021-02 [I,A]; H01L0021-02 [I,C]; H01L0021-20 [I,A];  
H01L0021-331 [I,A]; H01L0021-336 [I,A]; H01L0021-338  
[I,A]; H01L0021-70 [I,C]; H01L0021-762 [I,A]; H01L0027-12  
[I,A]; H01L0027-12 [I,C]; H01L0029-02 [I,C];  
H01L0029-161 [I,A]; H01L0029-66 [I,C]; H01L0029-737 [I,A]  
; H01L0029-778 [I,A]; H01L0029-786 [I,A]; H01L0029-812  
[I,A]; H01L0029-861 [I,A]; H01L0031-10 [I,A]; H01L0031-10  
[I,C]

BASIC ABSTRACT:

WO 2002033746 A1 UPAB: 20060119

NOVELTY - A relaxed silicon germanium layer on an insulator and a  
silicon germanium/silicon heterostructure are prepared by forming a  
relaxed epitaxial layer on a graded layer. A surface of the relaxed layer  
is smoothed to provide a specified surface roughness. A second substrate  
is selected and a top surface of the relaxed layer on a first substrate  
is bonded to second substrate.

DETAILED DESCRIPTION - Preparation of a relaxed silicon germanium  
(SiGe) layer on an insulator and a SiGe/Si heterostructure involves  
forming a graded silicon germanium-containing (Si1-xGex) epitaxial layer  
on a first single crystalline semiconductor substrate. A relaxed Si1-yGe  
epitaxial layer (30) is formed on the graded Si1-xGex layer. The surface  
of the relaxed layer is smoothed to provide a surface roughness of 0.3-1  
nm root mean square (RMS). A second substrate (80) with or without an  
insulator having a major surface with the surface roughness is selected.



The top surface of the relaxed layer on the first substrate is bonded to the second substrate. The bonding step includes annealing to form strong bonds across the bonding interface to form a single mechanical structure.

An INDEPENDENT CLAIM is included for a **multi-layer** substrate for use in integrated circuits comprising a silicon containing substrate, a silicon oxide layer on the silicon containing substrate, and a relaxed Si<sub>1-y</sub>Ge<sub>y</sub> layer on the silicon oxide layer.

USE - For preparing a relaxed silicon germanium layer on an insulator and a silicon germanium/silicon heterostructure.

ADVANTAGE - The method is capable of transferring a low defect SiGe layer onto a desirable substrate using the etch-back method but without any additional heavily doped etch-stop layer. The SiGe layer serves both as the layer over which the epitaxial strained Si/SiGe is grown and as an etch-stop layer. The method provides simplification of the strained Si/SiGe fabrication on the insulator. It improves the quality of the strained Si/SiGe or SiGe/Si heterostructure.

DESCRIPTION OF DRAWINGS - The figure is a cross section view of an epitaxially grown strained Si/SiGe layer or a p-i-n photodetector epitaxially grown on the smoothed Si<sub>1-y</sub>Ge<sub>y</sub> layer.

Relaxed Si<sub>1-y</sub>Ge<sub>y</sub> epitaxial layer (30)

Second substrate (80)

#### TECHNOLOGY FOCUS:

ELECTRONICS - Preferred Method: The method includes smoothing the upper surface of the relaxed layer on the second substrate so that additional epitaxial layers may be grown and removing the first substrate.

An encapsulation layer is formed on the surface of the relaxed SiGe layer of the first substrate and annealed at 400-900degreesC.

The smoothing step includes chemical-mechanical planarization to smooth the relaxed layer surface and provide a surface roughness of 0.3-1 nm RMS.

An insulator layer is formed on the second substrate for the formation of the strained Si/SiGe on **insulator** at 400-900degreesC.

A conducting layer is formed on the second substrate for the formation of the p-i-n SiGe/Si heterodiodes.

The insulator layer is formed by plasma enhanced chemical vapor deposition (PECVD), low pressure CVD, ultra high vacuum CVD or spin-on techniques. An intermediate agent layer may be used to enhance the bonding interface.

The annealing step includes thermal treatment cycles to form a strong bond at the bonded interface and heating to 100-800degreesC. It uses air, nitrogen or argon. The thermal treatment is furnace anneal and/or rapid thermal anneal (RTA). A highly wet etching process is used to remove Si substrate of the first substrate. It uses EPPW, potassium hydroxide or tetra-methyl ammonium hydroxide as wet etchant at 70-120degreesC.

Preferred Dimension: The low-defect relaxed layer on the second substrate has a thickness of 50-100 nm as determined by the layer structure formed on the first substrate.

INORGANIC CHEMISTRY - Preferred Materials: The epitaxial layer is Si<sub>1-y</sub>Ge<sub>y</sub>, silicon (Si), silicon carbide (SiC), germanium, germanium carbide or Si<sub>1-y</sub>Ge<sub>y</sub>C. The Si<sub>1-y</sub>Ge<sub>y</sub> material is selected with a value to allow absorption of light in the infrared range (less than 1  $\mu$ m wavelength). The encapsulation layer is made of Si, poly Si, silicon dioxide (SiO<sub>2</sub>) or silicon nitride (Si<sub>3</sub>N<sub>4</sub>).

The first substrate is Si, SiGe, SiGeC, SiC, gallium arsenide (GaAs) or indium phosphide (InP). The insulator layer includes SiO<sub>2</sub>,

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Si<sub>3</sub>N<sub>4</sub>, aluminum oxide, lithium niobate (LiNbO<sub>3</sub>) and/or low-k materials (where k is less than 3.2). The conducting layer includes heavily doped p+ Si or p+ poly Si. The second substrate is Si, SiGe, SiGeC, SiC, GaAs, InP, sapphire, LiNbO<sub>3</sub>, quartz, lead-lanthanum-zirconium-titanate. The intermediate agent layer is Ge, aluminum, tungsten, cobalt or titanium.

FILE SEGMENT:

CPI; EPI

MANUAL CODE:

CPI: L04-A01A; L04-A01C; L04-C01B

EPI: U11-C01J1; U11-C08A3

02/06/2007 10/710826 Doty

L28 ANSWER 6 OF 6 WPIX COPYRIGHT 2007 THE THOMSON CORP on STN  
ACCESSION NUMBER: 1994-308339 [38] WPIX  
DOC. NO. CPI: C1994-140593 [38]  
DOC. NO. NON-CPI: N1994-242537 [38]  
TITLE: Semiconductor device **multist**structure  
layer structure production method - by  
incorporating **silicon-germanium** layer  
above **insulation** layer and combining silicon  
germanium layer and severing insulation layer structure  
from silica film by cutting  
DERWENT CLASS: L03; U11  
INVENTOR: MATSUSHITA T; SAMEJIMA T; USUI S  
PATENT ASSIGNEE: (SONY-C) SONY CORP  
COUNTRY COUNT: 1

PATENT INFORMATION:

PATENT NO	KIND	DATE	WEEK	LA	PG	MAIN IPC
JP 06236975	A	19940823	(199438)*	JA	12[14]	H01L027-12

APPLICATION DETAILS:

PATENT NO	KIND	APPLICATION	DATE
JP 06236975	A	JP 1993-41763	19930208

PRIORITY APPLN. INFO: JP 1993-41763 19930208

INT. PATENT CLASSIF.:

IPC RECLASSIF.: H01L0021-02 [I,A]; H01L0021-02 [I,C]; H01L0021-70 [I,C];  
H01L0021-76 [I,A]; H01L0021-762 [I,A]; H01L0027-12 [I,A];  
H01L0027-12 [I,C]

BASIC ABSTRACT:

JP 06236975 A UPAB: 20050509

The multilayer structure consists of several dissimilar layers formed one above the other on a supporting substrate (20). The first layer above the supporting layer substrate is SiO<sub>2</sub> film (22). Next, is the insulation layer (14) which is above the SiO<sub>2</sub> film.

Next, Sil-XGeX layer (12) is formed above the insulation layer. Above the Sil-XGeX layer is the monocrystal silicon layer (10) originally present in the substrate. The multilayer structure is now cut along the interface between SiO<sub>2</sub> film and insulation layer. The semiconductor element is formed in Sil-XGeX layer. The layer after cutting is cleaned by suitable processes.

ADVANTAGE - Controls Sil-XGeX layer with high accuracy. Stops removal of semiconductor layer formation near boundary face of substrate.

FILE SEGMENT: CPI; EPI  
MANUAL CODE: CPI: L04-C10F; L04-C13  
EPI: U11-C08A6

02/06/2007 10/710826 Doty

L36 ANSWER 2 OF 20 KOREAPAT COPYRIGHT 2007 KIPI on STN  
ACCESSION NUMBER: 2005:021026 KOREAPAT ED 20050802  
TITLE: USE OF THIN SOI TO INHIBIT RELAXATION OF **SiGe**  
LAYERS AND METHOD OF FABRICATING **SGOI** SUBSTRATE  
MATERIALS  
TITLE LANGUAGE: English  
INVENTOR(S): BEDELL STEPHEN W.; CHEN HUAJIE; FOGEL KEITH E.; SADANA  
DAVENDRA K.  
PATENT ASSIGNEE(S): INTERNATIONAL BUSINESS MACHINES CORPORATION  
PATENT INFO TYPE: KRA Unexamined Patent Application  
PATENT INFO: KR 2005025261 A 20050314  
APPLICATION INFO: KR 2004-61937 20040806  
PRIORITY APPLN. INFO: US 2003-654232 20030903  
INT. PATENT CLASSIF:  
MAIN: H01L021-20  
SECONDARY H01L029-04  
H01L021-8238  
ABSTRACT: PURPOSE: A use of a thin SOI(Silicon On Insulator) to  
inhibit relaxation of **SiGe** layers is provided  
to fabricate an **SGOI(SiGe-On-Insulator)** substrate material having a  
metastable-strained **SiGe** layer by growing an  
**SiGe** layer on a high-quality SOI substrate.  
CONSTITUTION: A Ge-containing layer is formed on a  
surface of a top Si-containing layer having the thickness  
of 500 angstrom or less and being located on a barrier  
layer(12) that is resistant to Ge diffusion. The layers  
are heated at a temperature which permits inter-diffusion  
of Ge throughout the top Si-containing layer and the  
Ge-containing layer in order to form a substantially  
metastable **SiGe** layer(20) for preventing  
relaxation on the barrier layer.  
.COPYRGT. KIPO 2005

L36 ANSWER 3 OF 20 KOREAPAT COPYRIGHT 2007 KIPI on STN  
ACCESSION NUMBER: 2005:003746 KOREAPAT ED 20050517  
TITLE: METHOD FOR DEFECT REDUCTION BY OXIDATION OF SILICON FOR  
FABRICATING THIN, HIGH-QUALITY, AND SUBSTANTIALLY RELAXED  
**SiGe-ON-INSULATOR** SUBSTRATE MATERIALS  
BY USING SOI SUBSTRATE AS TEMPLATE  
TITLE LANGUAGE: English  
INVENTOR(S): CHEN, HUAJIE; BEDELL, STEPHEN W.; DOMENICUCCI, ANTHONY  
G.; FOGEL, KEITH E.; SADANA, DEVENDRA K.  
PATENT ASSIGNEE(S): INTERNATIONAL BUSINESS MACHINES CORPORATION  
PATENT INFO TYPE: KRA Unexamined Patent Application  
PATENT INFO: KR 2005003992 A 20050112  
APPLICATION INFO: KR 2004-39652 20040601  
PRIORITY APPLN. INFO: US 2003-610612 20030701  
INT. PATENT CLASSIF:  
MAIN: H01L021-20  
ABSTRACT: PURPOSE: A method for defect reduction by oxidation of  
silicon is provided to fabricate thin, high-quality, and  
substantially relaxed **SiGe-on-insulator**  
substrate materials by using an SOI substrate as a  
template.  
CONSTITUTION: A strained Ge-containing layer(16) is  
formed on a surface of a sacrificial single crystal Si  
layer(14). The sacrificial single crystal Si layer is  
present at a top of a barrier layer that is resistant to  
Ge diffusion. The layers are oxidized at a temperature  
that homogenizes Ge atoms throughout the sacrificial  
single crystal Si layer and the Ge-containing layer,  
relaxes the Ge-containing layer by creating dislocations  
that are injected predominately into the sacrificial  
single crystal Si layer, and consumes the sacrificial  
single crystal Si layer by internal oxidation thereby  
forming a substantially relaxed single crystal  
**SiGe** layer.  
.COPYRGT. KIPO 2005

L36 ANSWER 4 OF 20 KOREAPAT COPYRIGHT 2007 KIPI on STN  
ACCESSION NUMBER: 2004:088452 KOREAPAT ED 20050404  
TITLE: METHOD OF FABRICATING SUBSTANTIALLY RELAXED, HIGH-QUALITY  
SiGe CRYSTAL LAYER OVER INSULATING LAYER BY  
COMBINING ASPECTS OF SILICON-ON-INSULATOR FORMATION WITH  
INTER-DIFFUSION OF Ge-CONTAINING LAYER  
TITLE LANGUAGE: English  
INVENTOR(S): BEDELL, STEPHEN W.; FOGEL, KEITH E.; SADANA, DEVENDRA K.;  
SHAHIDI; GHAVAM G.  
PATENT ASSIGNEE(S): INTERNATIONAL BUSINESS MACHINES CORPORATION.  
PATENT INFO TYPE: KRA Unexamined Patent Application  
PATENT INFO: KR 2004104360 A 20041210  
APPLICATION INFO: KR 2004-30221 20040429  
PRIORITY APPLN. INFO: US 2003-448947 20030530  
INT. PATENT CLASSIF:  
MAIN: H01L021-20  
ABSTRACT: PURPOSE: A method of producing a substantially relaxed  
and high-quality SiGe-on-insulator  
substrate material is provided to form thin,  
high-quality, and substantially relaxed SiGe  
-on-insulator substrate materials.  
CONSTITUTION: Ions are implanted into an Si-containing  
substrate(10) to form an implant rich region having an  
ion concentration that is sufficient to act as a  
diffusion barrier to Ge. The implant rich region has a  
surface layer of the Si-containing substrate located  
thereon. A Ge-containing layer is formed on the top of  
the implanted Si-containing substrate. The substrate is  
heated at a temperature which permits formation of a  
diffusion barrier layer and inter-diffusion of Ge  
throughout the Ge-containing layer and the surface layer  
of Si-containing substrate located above the implant rich  
region. A substantially relaxed SiGe layer(20)  
is formed on the top of the diffusion barrier layer.  
.COPYRGT. KIPO 2005



L36 ANSWER 6 OF 20 KOREAPAT COPYRIGHT 2007 KIPI on STN  
ACCESSION NUMBER: 2003:032160 KOREAPAT ED 20040819  
TITLE: METHOD FOR FORMING SOI SUBSTRATE  
TITLE LANGUAGE: English  
INVENTOR(S): BAE, GEUM JONG; FUJIHARA, KAZUYUKI; KIM, SANG SU; LEE,  
HWA SEONG; LEE, JEONG IL; LEE, NAE IN  
PATENT ASSIGNEE(S): SAMSUNG ELECTRONICS CO., LTD.  
PATENT INFO TYPE: KRA Unexamined Patent Application  
PATENT INFO: KR 2003045936 A 20030612  
APPLICATION INFO: KR 2001-75864 20011203  
PRIORITY APPLN. INFO: KR 2001-75864 \* 20011203  
INT. PATENT CLASSIF:  
MAIN: H01L021-20  
ABSTRACT: PURPOSE: A method for forming an SOI(strained  
**silicon on Silicon-germanium**  
On Insulator) substrate is provided to enhance  
the mobility of the current carrier by forming a strained  
silicon layer on a surface of an SOI layer including  
germanium.  
CONSTITUTION: A relaxed **silicon**  
**germanium** layer is formed on the first silicon  
substrate by using an epitaxial growth method. A porous  
**silicon germanium** layer is formed on  
the relaxed **silicon germanium** layer.  
A **silicon germanium** epitaxial  
layer(118) is formed on the porous **silicon**  
**germanium** layer. An oxide layer(122) is formed on  
the second silicon substrate(124). A front surface of the  
first silicon substrate and a front surface of the second  
substrate are adhered to each other. A **silicon**  
**germanium** epitaxial layer is formed by removing  
material layers from an upper portion of the porous  
**silicon germanium** layer. A strained  
silicon epitaxial layer(126) is formed on the  
**silicon germanium** epitaxial layer.  
.COPYRGT. KIPO 2003

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L36 ANSWER 7 OF 20 JAPIO (C) 2007 JPO on STN

ACCESSION NUMBER: 1988-015484 JAPIO

TITLE: THIN-FILM ELECTRIC CONDUCTOR OF MIXED **SILICON**  
/**GERMANIUM**/ GOLD CRYSTAL

INVENTOR: TENMA TAKESHI; KOTADO SETSUO

PATENT ASSIGNEE(S): ANRITSU CORP

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 63015484	A	19880122	Showa	H01L035-14

APPLICATION INFORMATION

STN FORMAT: JP 1986-159325 19860707

ORIGINAL: JP61159325 Showa

PRIORITY APPLN. INFO.: JP 1986-159325 19860707

SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined  
Applications, Vol. 1988

INT. PATENT CLASSIF.:

MAIN: H01L035-14

SECONDARY: H01L029-84

ABSTRACT:

PURPOSE: To obtain a large value of a dark conductivity and form a compact resistor on an insulating substrate by treating vapor deposited gold with heat using an electric furnace after forming a thin film of mixed amorphous **silicon/ germanium** on the insulating substrate.

CONSTITUTION: A coning 7059 glass is used as an insulating substrate 1 and a gold thin film 3 is obtained by taking the following steps: (1) Oxide films are accumulated on thin amorphous **silicon/ germanium** films 2 by a plasma CVD process. (2) the accumulated oxide films are treated by a vapor deposition process after removing the oxide films by using an etching solution, a mixture of hydrofluoric acid, nitric acid, and acetic acid. In such a case, gold is diffused into the thin amorphous **silicon/germanium** films when the above thin films are treated with heat using an electric furnace at a temperature of 700&deg;C for an hour in an atmosphere of nitrogen and accordingly a dark conductivity increases. Even when the dark conductivity gets more than 200 S.cm<SP>-1</SP>, Seebeck coefficient is more than 80&sim;130 &mu;V/K and as a result, an electric conductor can be used to compose high-efficiency thermocouple, high-frequency power sensor, infrared sensor, temperature sensor, and the like.

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L36 ANSWER 11 OF 20 JAPIO (C) 2007 JPO on STN  
ACCESSION NUMBER: 2006-032962 JAPIO  
TITLE: METHOD OF FORMING RELAXED **SiGe** LAYER  
INVENTOR: BEDELL STEPHEN W; CHEN HUAJIE; FOGEL KEITH E; SADANA  
DEVENDRA K; SHAHIDI GHAVAM G  
PATENT ASSIGNEE(S): INTERNATL BUSINESS MACH CORP <IBM>  
PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 2006032962	A	20060202	Heisei	

APPLICATION INFORMATION

STN FORMAT: JP 2005-204182 20050713  
ORIGINAL: JP2005204182 Heisei  
PRIORITY APPLN. INFO.: US 2004-890765 20040714  
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined  
Applications, Vol. 2006

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a method for suppressing the formation of flat surface defects, such as stacking faults and microtwins in a relaxed **SiGe** alloy layer.

SOLUTION: There is disclosed the method of manufacturing a substantially-relaxed **SiGe** alloy layer, in which flat surface defect density is decreased. The method comprises the steps of forming a strained Ge-containing layer on the front surface of an Si-containing substrate, implanting ions into the interface of the Ge-containing layer/the Si-containing substrate or under the interface, and forming the substantially-relaxed **SiGe** alloy layer, in which the flat surface defect density is decreased. Further, there are also provided a substantially relaxed **SiGe-on-insulator**, having an **SiGe** layer in which the flat surface defect density is decreased, and a heterostructure comprising the insulator.

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L36 ANSWER 13 OF 20 JAPIO (C) 2007 JPO on STN

ACCESSION NUMBER: 2005-109447 JAPIO

TITLE: METHOD FOR MANUFACTURING STRAIN-RELAXED  
SILICON-GERMANIUM ON  
INSULATOR VIA DISLOCATED LAYER BY REDUCING  
STRESS

INVENTOR: MAA JER-SHEN; LEE JONG JAN; TWEET DOUGLAS J; SHIEN TEN  
SUU

PATENT ASSIGNEE(S): SHARP CORP

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 2005109447	A	20050421	Heisei	H01L021-20

APPLICATION INFORMATION

STN FORMAT: JP 2004-247613 20040826

ORIGINAL: JP2004247613 Heisei

PRIORITY APPLN. INFO.: US 2003-677005 20030930

SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined  
Applications, Vol. 2005

INT. PATENT CLASSIF.:

MAIN: H01L021-20

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a method for manufacturing strain-relaxed **silicon-germanium**, by which omission of **SiGe** deposition step and the subsequent complicated CMP (chemical mechanical planarization) step is possible.

SOLUTION: The method for manufacturing the strain-relaxed **silicon-germanium** layer on an insulator includes a step in which **silicon/silicon-germanium** is formed, a step in which hydrogen ions are injected into a silicon substrate, a step in which the **silicon/silicon-germanium** is combined with an insulator substrate, a first heat annealing step in which a couplet is divided by heat annealing, a step in which silicon portion and the **SiGe** layer are eliminated, by patterning and etching of **silicon-germanium** portion on the insulator, a step in which residual silicon layer is eliminated by etching of the **silicon-germanium** portion on the insulator, a second heat annealing step in which the **silicon-germanium** portion on the insulator is annealed, and a step in which strained silicon layer is deposited around the **SiGe** layer.

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L36 ANSWER 14 OF 20 JAPIO (C) 2007 JPO on STN

ACCESSION NUMBER: 2005-101568 JAPIO

TITLE: METHOD FOR MAKING RELAXED SILICON  
GERMANIUM ON INSULATOR THROUGH LAYER  
DISPLACEMENT

INVENTOR: MAA JER-SHEN; LEE JONG JAN; TWEET DOUGLAS J; SHIEN TEN  
SUU

PATENT ASSIGNEE(S): SHARP CORP

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 2005101568	A	20050414	Heisei	H01L021-20

APPLICATION INFORMATION

STN FORMAT: JP 2004-241711 20040820

ORIGINAL: JP2004241711 Heisei

PRIORITY APPLN. INFO.: US 2003-665944 20030919

SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined  
Applications, Vol. 2005

INT. PATENT CLASSIF.:

MAIN: H01L021-20

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a method for making an SiGe  
layer which coats an insulator.

SOLUTION: A layer of SiGe is deposited on a substrate and  
implanted with ions to form a depletion region within a SiGe  
material below its surface. The SiGe layer is then allowed to  
contact and couple to an insulator on a second substrate for patterning  
and displacement. After contacting and coupling, the structure is annealed  
to separate the SiGe layer along the depletion region. The  
annealing for separation makes the SiGe layer relaxed. The  
SiGe layer may be further relaxed by using additional annealing at  
higher temperatures. A strained silicon layer may be epitaxially deposited  
on the relaxed SiGe structure which has been finally produced on  
the insulator. Another method for epitaxially depositing a silicon layer  
over the SiGe layer prior to patterning is provided.

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02/06/2007 10/710826 Doty

L36 ANSWER 15 OF 20 JAPIO (C) 2007 JPO on STN

ACCESSION NUMBER: 2005-044892 JAPIO

TITLE: METHOD FOR MANUFACTURING SGOI SUBSTRATE, AND  
METHOD FOR MANUFACTURING DISTORTION SOI SUBSTRATE

INVENTOR: TEZUKA TSUTOMU; TAKAGI SHINICHI; MIZUNO TOMOHISA

PATENT ASSIGNEE(S): TOSHIBA CORP

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 2005044892	A	20050217	Heisei	H01L027-12

APPLICATION INFORMATION

STN FORMAT: JP 2003-201038 20030724

ORIGINAL: JP2003201038 Heisei

PRIORITY APPLN. INFO.: JP 2003-201038 20030724

SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined  
Applications, Vol. 2005

INT. PATENT CLASSIF.:

MAIN: H01L027-12

SECONDARY: H01L021-20; H01L021-762

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a method which can manufacture a distortion SOI substrate wherein an SiGe layer having Ge composition of high enough is contained and dislocation density is low.  
SOLUTION: The method for manufacturing the distortion SOI substrate contains a process wherein a laminate structure substrate in which an insulating film (2), an Si crystal layer (3) and a distortion SiGe crystal layer (4) are laminated on a substrate (1) is subjected to heat treatment in oxidizing atmosphere, an oxide film (6) is formed on a surface, composition of the distortion SiGe crystal layer (4) and the Si crystal layer (3) are made uniform, and a lattice relaxation SiGe crystal layer (7) whose Ge composition is made greater than that of the SiGe crystal layer of original is formed, a process wherein the oxide film (6) formed on the surface is eliminated and the exposed lattice relaxation SiGe crystal layer (7) is thinned, and a process wherein a distortion Si crystal layer (9) is epitaxially grown on the thinned lattice relaxation SiGe crystal layer (7).

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L36 ANSWER 16 OF 20 JAPIO (C) 2007 JPO on STN  
ACCESSION NUMBER: 2005-026681 JAPIO  
TITLE: DEFECT CONTROL BY OXIDATION OF SILICON  
INVENTOR: BEDELL STEPHEN W; CHEN HUAJIE; DOMENICUCCI ANTHONY G;  
FOGEL KEITH E; SADANA DEVENDRA K  
PATENT ASSIGNEE(S): INTERNATL BUSINESS MACH CORP <IBM>  
PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 2005026681	A	20050127	Heisei	H01L027-12

APPLICATION INFORMATION

STN FORMAT: JP 2004-183839 20040622  
ORIGINAL: JP2004183839 Heisei  
PRIORITY APPLN. INFO.: US 2003-610612 20030701  
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined  
Applications, Vol. 2005

INT. PATENT CLASSIF.:

MAIN: H01L027-12

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a method for manufacturing an **SiGe-on-insulator** substrate material substantially relaxed, of high quality, and capable of being used as a template for strained-silicon.

SOLUTION: The SOI substrate having an ultra-thin top Si layer is used as the template for compressive strain **SiGe** growth. When an **SiGe** layer is relaxed at an enough temperature, the property of its dislocation movement is such that strain release defect moves down into the thin Si layer when an embedded oxide shows semi-viscosity behavior. The thin Si layer is consumed by oxidation of an interface of the thin Si with the embedded oxide. This can be performed by using inner oxidation at a high temperature. Therefore, the role of the original thin Si layer is to use the inner oxidation and subsequently to act as a sacrificial defective sink capable of being consumed during an **SiGe** alloy being relaxed.

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L36 ANSWER 18 OF 20 JAPIO (C) 2007 JPO on STN

ACCESSION NUMBER: 2004-214629 JAPIO

TITLE: PATTERNED STRAINED (STRESS DEFORMATION) SILICON FOR  
HIGH-PERFORMANCE CIRCUIT

INVENTOR: SADANA DEVENDRA K; BEDELL STEPHEN W; CHEN TZE-CHIANG;  
CHOE KWANG SU; FOGEL KEITH E

PATENT ASSIGNEE(S): INTERNATL BUSINESS MACH CORP <IBM>

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 2004214629	A	20040729	Heisei	H01L027-12

APPLICATION INFORMATION

STN FORMAT: JP 2003-396383 20031126

ORIGINAL: JP2003396383 Heisei

PRIORITY APPLN. INFO.: US 2003-336147 20030102

SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined  
Applications, Vol. 2004

INT. PATENT CLASSIF.:

MAIN: H01L027-12

SECONDARY: H01L021-20; H01L021-76; H01L021-762

ABSTRACT:

PROBLEM TO BE SOLVED: To develop a new improved method for forming a relaxed SiGe-on-insulator substrate material which is thermodynamically stable with respect to the generation of a defect. SOLUTION: Silicon to which tensile stress is applied is formed by epitaxially growing over the whole SiGe alloy layer. Silicon to which compressive stress is applied is formed by epitaxially growing over the whole porous silicon. A method of converting a patterned SOI region into patterned an SGOI (silicon-germanium ON oxide) by a SiGe/SOI heat mixing process for farther reinforcing the performance of a logic circuit in a padded DRAM is described in a preferred embodiment. The SGOI region in which Si is strained acts as a template for succeeding Si growth so that electrons and holes in the Si have higher mobilities.

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L48 ANSWER 1 OF 2 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2004:7995119 INSPEC  
DOCUMENT NUMBER: B2004-07-2550E-034  
TITLE: Advanced SOI substrate manufacturing  
AUTHOR: Mazure, C.; Celler, G.K.; Maleville, C.; Cayrefourcq, I. (Soitec SA, Crolles, France)  
SOURCE: 2004 International Conference on Integrated Circuit Design and Technology (IEEE Cat. No.04EX866), 2004, p. 105-11 of ix+368 pp., 15 refs.  
ISBN: 0 7803 8528 4  
Price: 0-7803-8528-4/04/\$20.00  
Published by: IEEE, Piscataway, NJ, USA  
Conference: 2004 International Conference on Integrated Circuit Design and Technology, Austin, TX, USA, 17-20 May 2004  
Sponsor(s): IEEE Central Texas Sect.; Japan Soc. Appl. Phys  
DOCUMENT TYPE: Conference; Conference Article  
TREATMENT CODE: Practical  
COUNTRY: United States  
LANGUAGE: English  
ABSTRACT: 300 mm SOI wafers with sub-100nm thick active Si layers are currently produced in large quantities and used in advanced microprocessor circuits. To further enhance the performance of the next generation of devices, strained Si layers on insulator are being developed. The lattice mismatch between silicon and SiGe alloys, combined with layer transfer through the Smart Cut® technology allow forming two types of strained Si - strained Si on SiGe on insulator, known as SGOI, and strained Si directly on insulator, known as sSOI. Fabrication methods and wafer characteristics for SOI, SGOI, and sSOI are discussed here  
CLASSIFICATION CODE: B2550E Surface treatment (semiconductor technology); B2530F Metal-insulator-semiconductor structures; B2550B Semiconductor doping; B2570D CMOS integrated circuits  
CONTROLLED TERM: CMOS integrated circuits; etching; ion implantation; oxidation; semiconductor superlattices; silicon-on-insulator; substrates; surface cleaning; wafer bonding  
SUPPLEMENTARY TERM: advanced SOI substrate manufacturing; SOI wafers; next generation devices; strained layers; lattice mismatch; layer transfer; Smart Cut technology; wafer characteristics; high performance CMOS applications; wafer bonding; ion implantation induced weakening; wet cleaning; oxidation; ultrathin wafers; film thickness uniformity; selective wet etch; Si-SiGe; Si  
CHEMICAL INDEXING: Si-SiGe int, SiGe int, Ge int, Si int, SiGe bin, Ge bin, Si bin, Si el; Si int, Si el  
ELEMENT TERMS: Ge\*Si; Ge sy 2; sy 2; Si sy 2; SiGe; Si cp; cp; Ge cp; Ge; Si

L51 ANSWER 1 OF 1 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2003:7710097 INSPEC  
DOCUMENT NUMBER: A2003-19-7320A-001; B2003-09-2560R-050  
TITLE: Hole mobility enhancements in nanometer-scale strained-silicon heterostructures grown on Ge-rich relaxed Si<sub>1-x</sub>Ge<sub>x</sub>  
AUTHOR: Lee, M.L.; Fitzgerald, E.A. (Dept. of Mater. Sci. & Eng., Massachusetts Inst. of Technol., Cambridge, MA, USA)  
SOURCE: Journal of Applied Physics (15 Aug. 2003), vol.94, no.4, p. 2590-6, 29 refs.  
CODEN: JAPIAU, ISSN: 0021-8979  
SICI: 0021-8979(20030815)94:4L:2590:HMEN;1-V  
Price: 0021-8979/2003/94(4)/2590(7)/\$20.00  
Doc.No.: S0021-8979(03)03916-1  
Published by: AIP, USA  
DOCUMENT TYPE: Journal  
TREATMENT CODE: Theoretical; Experimental  
COUNTRY: United States  
LANGUAGE: English  
ABSTRACT: Although strained-silicon (X220A-Si) p-type metal-oxide-semiconductor field-effect transistors (p-MOSFETs) demonstrate enhanced hole mobility compared to bulk Si devices, the enhancement has widely been observed to degrade at large vertical effective fields. We conjecture that the hole wave function in X220A-Si heterostructures spreads out over distances of 10 nm, even at large inversion densities, due to the strain-induced reduction of the out-of-plane effective mass. Relevant experimental and theoretical studies supporting this argument are presented. We further hypothesize that by growing layers thinner than the hole wave function itself, inversion carriers can be forced to occupy and hybridize the valence bands of different materials. In this article, we show that p-MOSFETs with thin (i.e., <3 nm) X220A-Si layers grown on Ge-rich Si<sub>1-x</sub>Ge<sub>x</sub> buffers exhibit markedly different mobility enhancements from prior X220A-Si p-MOSFETs. Devices fabricated on a thin X220A-Si layer grown on relaxed Si<sub>0.3</sub>Ge<sub>0.7</sub> demonstrate hole mobility enhancements that increase with gate overdrive, peaking at a value of nearly 3 times. In other devices where the channel region consists of a periodic X220A-Si/relaxed Si<sub>0.3</sub>Ge<sub>0.7</sub> digital alloy, a nearly constant mobility enhancement of 2.0 was observed over inversion densities ranging from 3 to 14×10<sup>12</sup>/cm<sup>2</sup>  
CLASSIFICATION CODE: A7320A Surface states, band structure, electron density of states; A7125J Effective mass and g-factors (condensed matter electronic structure); B2560R Insulated gate field effect transistors  
CONTROLLED TERM: effective mass; elemental semiconductors; Ge-Si alloys; hole mobility; internal stresses; MOSFET; semiconductor device measurement; semiconductor materials; silicon; stress relaxation; valence bands; wave functions  
SUPPLEMENTARY TERM: hole mobility enhancement; nanometer-scale

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CHEMICAL INDEXING:

strained-silicon heterostructures; Ge-rich relaxed  
Si<sub>1-x</sub>Ge<sub>x</sub>; p-type metal-oxide-semiconductor  
field-effect transistors; p-MOSFETs; enhanced hole  
mobility; hole wave function; out-of-plane effective  
mass; layer thickness; valence bands; gate overdrive;  
inversion density; 10 nm; Si; Si<sub>0.3</sub>Ge<sub>0.7</sub>

PHYSICAL PROPERTIES:

Si int, Si el; Si<sub>0.3</sub>Ge<sub>0.7</sub> int, Ge<sub>0.7</sub> int, Si<sub>0.3</sub>  
int, Ge int, Si int, Si<sub>0.3</sub>Ge<sub>0.7</sub> bin, Ge<sub>0.7</sub> bin, Si<sub>0.3</sub>  
bin, Ge bin, Si bin

ELEMENT TERMS:

size 1.0E-08 m  
Si; Ge\*Si; Ge sy 2; sy 2; Si sy 2; Si<sub>1-x</sub>Ge<sub>x</sub>; Si cp;  
cp; Ge cp; Ge; Si<sub>0.3</sub>Ge; Si<sub>0.3</sub>Ge<sub>0.7</sub>

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L60 ANSWER 12 OF 55 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2005:8348149 INSPEC  
DOCUMENT NUMBER: B2005-05-7230C-047  
TITLE: Fabrication of p-i-n Si<sub>0.5</sub>Ge<sub>0.5</sub> photodetectors on  
**SiGe-on-insulator substrates**  
AUTHOR: Koh, S.; Sawano, K.; Shiraki, Y.; (Dept. of Appl.  
Phys., Tokyo Univ., Japan), Usami, N.; Nakajima, K.;  
Huang, X.; Uda, S.  
SOURCE: 2004 1st IEEE International Conference on Group IV  
Photonics (IEEE Cat. No.04EX849), 2004, p. 61-3 of 196  
pp., 6 refs.  
ISBN: 0 7803 8474 1  
Price: 0-7803-8474-1/04/\$20.00  
Published by: IEEE, Piscataway, NJ, USA  
Conference: 2004 1st IEEE International Conference on  
Group IV Photonics, Hong Kong, China, 29 Sept.-1 Oct.  
2004  
DOCUMENT TYPE: Conference; Conference Article  
TREATMENT CODE: Practical; Experimental  
COUNTRY: United States  
LANGUAGE: English  
ABSTRACT: This study demonstrates the fabrication and evaluation  
of a Si<sub>0.5</sub>Ge<sub>0.5</sub> p-i-n photodetector for 1.3 μm  
light detection on **SiGe-on-insulator**  
(**SGOI**) **substrates** with the Ge  
content of 0.5. Gas-source-MBE grown **SiGe**  
heterostructures on **SGOI substrates**  
are promising systems not only for high-speed  
**SiGe** hetero-devices, such as strained-  
**Si** and strained-**Ge MOSFETs**  
, but also for Si-based optoelectronic integrated  
circuits (OEIC's)  
CLASSIFICATION CODE: B7230C Photodetectors; B4250 Photoelectric devices;  
B0520D Vacuum deposition  
CONTROLLED TERM: **Ge-Si** alloys; molecular beam  
epitaxial growth; p-i-n photodiodes; photodetectors;  
semiconductor growth  
SUPPLEMENTARY TERM: photodetector fabrication; p-i-n photodetectors;  
Si<sub>0.5</sub>Ge<sub>0.5</sub> photodetectors; **SiGe-on-insulator**  
substrates; gas-source-MBE growth; **SiGe**  
heterostructures; high-speed **SiGe** heterodevices;  
strained-Si MOSFET; strained-Ge MOSFET; Si-based  
optoelectronic integrated circuits; 1.3 μm;  
Si<sub>0.5</sub>Ge<sub>0.5</sub>  
CHEMICAL INDEXING: **Si<sub>0.5</sub>Ge<sub>0.5</sub> int, Ge<sub>0.5</sub> int, Si<sub>0.5</sub> int, Ge int, Si**  
**int, Si<sub>0.5</sub>Ge<sub>0.5</sub> bin, Ge<sub>0.5</sub> bin, Si<sub>0.5</sub> bin, Ge bin, Si**  
**bin; Ge sur, Si sur, Ge ss, Si ss**  
PHYSICAL PROPERTIES: wavelength 1.3E-06 m  
ELEMENT TERMS: **Ge\*Si; Ge sy 2; sy 2; Si sy 2; Ge-Si; Ge; SiGe; Si cp;**  
**cp; Ge cp; Si; Si<sub>0.5</sub>Ge; Si<sub>0.5</sub>Ge<sub>0.5</sub>**



L60 ANSWER 13 OF 55 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2005:8304125 INSPEC  
DOCUMENT NUMBER: A2005-07-8115N-001; B2005-04-0520-003  
TITLE: **SiGe-on-insulator** and Ge-on-insulator substrates fabricated by Ge-condensation technique for high-mobility channel **CMOS** devices  
AUTHOR: Tezuka, T.; Mizuno, T.; Sugiyama, N.; Nakaharai, S.; Moriyama, Y.; Usuda, K.; Numata, T.; Hirashita, N.; (MIRAI-ASET, Kawasaki, Japan), Maeda, T.; Takagi, S.; Miyamura, Y.; Toyoda, E.  
SOURCE: High-Mobility Group-IV Materials and Devices (Materials Research Society Symposium Proceedings Vol.809), 2004, p. 65-75 of xii+304 pp., 18 refs. Editor(s): Caymax, M.; Rim, K.; Zaima, S.; Kasper, E.; Fichtner, P.F.P. Published by: Materials Research Society, Warrendale, PA, USA  
Conference: High-Mobility Group-IV Materials and Devices, San Francisco, CA, USA, 13-15 April 2004  
DOCUMENT TYPE: Conference; Conference Article  
TREATMENT CODE: Experimental  
COUNTRY: United States  
LANGUAGE: English  
ABSTRACT: A new fabrication method of **SiGe-on-insulator (SGOI)** and Ge-on-insulator (GOI) structures are presented as well as the application to high-mobility channel **CMOS** devices. This method, the Ge-condensation technique, consists of epitaxial growth of a **SiGe** layer with a low Ge fraction on an SOI substrate and successive oxidation at high temperatures, which can be incorporated in conventional **CMOS** processes. During the oxidation, Ge atoms are pushed out from the oxide layer and condensed in the remaining **SiGe** layer. The interface between the Si and **SiGe** layers disappeared due to the interdiffusion of Si and Ge atoms. Eventually, an **SGOI** layer with a higher Ge fraction is formed on the buried oxide layer. The Ge fraction in the **SGOI** layer can be controlled by the oxidation time because the total amount of Ge atoms in the **SGOI** layer is conserved throughout the oxidation process. We found that the lattice relaxation in the **SGOI** layer also can be controlled through the initial **SiGe** thickness. P- and n-type strained SOI **MOSFETs**, which were fabricated on relaxed **SGOI** substrates formed by this technique, exhibited mobility enhancement of 50% and 80%, respectively. **CMOS** ring oscillators comprised of the **MOSFETs** exhibited reduction in the propagation delay of 70%-30% compared to a conventional SOI-**CMOS** device. Ultrathin-body strained **SGOI** p**MOSFETs** with high Ge fraction and surface channels were also fabricated by this technique. These devices exhibited hole-mobility

enhancement factors up to 2.3. Furthermore, Ge-on-insulator (GOI) structures with thicknesses less than 10 nm were realized for ultrathin body GOI-CMOS applications by using the Ge-condensation technique. In conclusion, the Ge-condensation technique is a promising technique for fabricating various types of high-mobility channel-on-insulator devices

CLASSIFICATION CODE:

A8115N Thin film growth from solid phases; A6855 Thin film growth, structure, and epitaxy; A6470F Liquid-vapour transitions; A7340Q Electrical properties of metal-insulator-semiconductor structures; A7220F Low-field transport and mobility; piezoresistance (semiconductors/insulators); A8160C Surface treatment and degradation in semiconductor technology; A6630N Chemical interdiffusion in solids; A7360P Electrical properties of other inorganic semiconductors (thin films/low-dimensional structures); B0520 Thin film growth and epitaxy; B2530F Metal-insulator-semiconductor structures; B2560R Insulated gate field effect transistors; B2520M Other semiconductor materials; B2550E Surface treatment (semiconductor technology)

CONTROLLED TERM:

buried layers; chemical interdiffusion; condensation; electron mobility; Ge-Si alloys; hole mobility; MIS structures; MOSFET; oscillators; oxidation; semiconductor epitaxial layers; semiconductor growth; semiconductor materials; silicon-on-insulator; solid phase epitaxial growth

SUPPLEMENTARY TERM:

SiGe-on-insulator substrate; Ge-on-insulator substrate; SOI substrate; SiGe-on-insulator structure; Ge-on-insulator structure; Ge condensation method; high mobility channel CMOS devices; SiGe layer epitaxial growth; oxidation; Si atoms; Ge atoms; Ge fraction; interdiffusion; buried oxide layer; lattice relaxation; p type strained SOI MOSFET; n type strained SOI MOSFET; CMOS ring oscillators; propagation delay; hole mobility; surface channels; high mobility channel-on-insulator devices; condensation technique; 10 nm; Si-SiO<sub>2</sub>; Ge-SiO<sub>2</sub>; SiGe-SiO<sub>2</sub>

CHEMICAL INDEXING:

Si-SiO<sub>2</sub> int, SiO<sub>2</sub> int, O<sub>2</sub> int, Si int, O int, SiO<sub>2</sub> bin, O<sub>2</sub> bin, Si bin, O bin, Si el; Ge-SiO<sub>2</sub> int, SiO<sub>2</sub> int, Ge int, O<sub>2</sub> int, Si int, O int, SiO<sub>2</sub> bin, O<sub>2</sub> bin, Si bin, O bin, Ge el; SiGe-SiO<sub>2</sub> int, SiGe int, SiO<sub>2</sub> int, Ge int, O<sub>2</sub> int, Si int, O int, SiGe bin, SiO<sub>2</sub> bin, Ge bin, O<sub>2</sub> bin, Si bin, O bin

PHYSICAL PROPERTIES:

size 1.0E-08 m

ELEMENT TERMS:

Si; Ge; O\*Si; SiO<sub>2</sub>; Si cp; cp; O cp; Ge\*O\*Si; Ge sy 3; sy 3; O sy 3; Si sy 3; Ge-SiO<sub>2</sub>; SiO; O; Ge-SiO; Ge\*Si; Ge sy 2; sy 2; Si sy 2; SiGe; Ge cp; P

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L60 ANSWER 14 OF 55 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2005:8291615 INSPEC  
DOCUMENT NUMBER: B2005-03-2560X-015  
TITLE: Fabrication and characterization of a germanium quantum-dot transistor formed by selective oxidation of **SiGe/Si-on-insulator**  
AUTHOR: Liao, W.M.; Lin, S.W.; Tseng, S.S.; Lin, C.K.; Kuo, M.T.; Li, P.W. (Dept. of Electr. Eng., Nat. Central Univ., Chung-li, Taiwan)  
SOURCE: Amorphous and Nanocrystalline Silicon Science and Technology-2004 (Materials Research Symposium Proceedings Vol.808), 2004, p. 11-16 of xix+735 pp., 14 refs.  
Editor(s): Ganguly, G.; Kondo, M.Schiff E.A.; Carius, R.; Biswas, R.  
Published by: Materials Research Soc, Warrendale, PA, USA  
Conference: Amorphous and Nanocrystalline Silicon Science and Technology-2004, San Francisco, CA, USA, 13-16 April 2004  
DOCUMENT TYPE: Conference; Conference Article  
TREATMENT CODE: Practical; Experimental  
COUNTRY: United States  
LANGUAGE: English  
ABSTRACT: A simple and **CMOS**-compatible fabrication method for germanium (Ge) single-electron transistors (SET's) is proposed, in which the Ge quantum dots (QDs) are naturally formed by selective oxidation of Si<sub>0.95</sub>Ge<sub>0.05</sub>/Si wires on a silicon-on-insulator substrate. Clear Coulomb-blockade oscillations, Coulomb staircase, and negative differential conductances are experimentally observed at room temperature. The current-voltage characteristics of Ge SET's indicate that the addition energy of Ge QDs is about 130 meV and the Ge QD's diameter is about 7.7 nm, which agrees well with the transmission electron microscopy observation and numerical calculation  
CLASSIFICATION CODE: B2560X Quantum interference devices; B2550E Surface treatment (semiconductor technology)  
CONTROLLED TERM: Coulomb blockade; elemental semiconductors; **Ge-Si** alloys; oxidation; semiconductor materials; semiconductor quantum dots; silicon; silicon-on-insulator; single electron transistors; transmission electron microscopy  
SUPPLEMENTARY TERM: germanium quantum dot transistor; oxidation; SiGe-Si wires; silicon on insulator substrate; CMOS; single electron transistors; Coulomb blockade oscillations; negative differential conductances; room temperature; current-voltage curves; transmission electron microscopy; SiGe-Si-on-insulator; 293 to 298 K; 7.7 nm; Si<sub>0.95</sub>Ge<sub>0.05</sub>-Si; Si-SiO<sub>2</sub>  
CHEMICAL INDEXING: Si<sub>0.95</sub>Ge<sub>0.05</sub>-Si int, Si<sub>0.95</sub>Ge<sub>0.05</sub> int, Ge<sub>0.05</sub> int, Si<sub>0.95</sub> int, Ge int, Si int, Si<sub>0.95</sub>Ge<sub>0.05</sub> bin, Ge<sub>0.05</sub> bin, Si<sub>0.95</sub> bin, Ge bin, Si bin, Si el; SiSiO<sub>2</sub> sur, SiO<sub>2</sub> sur, O<sub>2</sub> sur, Si sur, O sur, SiSiO<sub>2</sub> ss, SiO<sub>2</sub> ss, O<sub>2</sub> ss, Si ss, O ss  
PHYSICAL PROPERTIES: temperature 2.93E+02 to 2.98E+02 K; size 7.7E-09 m

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L60 ANSWER 15 OF 55 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2005:8281025 INSPEC  
DOCUMENT NUMBER: B2005-03-2560R-128  
TITLE: 300 mm **SGOI**/strain-Si for high-performance  
**CMOS**  
AUTHOR: Reznicek, A.; Bedell, S.W.; Hovel, H.J.; Fogel, K.E.;  
Ott, J.A.; Mitchell, R.; Sadana, D.K. (IBM Thomas J.  
Watson Res. Center, Yorktown Heights, NY, USA)  
SOURCE: 2004 IEEE International SOI Conference (IEEE Cat.  
No.04CH37573), 2004, p. 37-8 of xv+216 pp., 3 refs.  
ISBN: 0 7803 8497 0  
Price: 0 7803 8497 0/2004/\$20.00  
Published by: IEEE, Piscataway, NJ, USA  
Conference: 2004 IEEE International SOI Conference,  
Charleston, SC, USA, 4-7 Oct. 2004  
Sponsor(s): IEEE Electron Devices Soc  
DOCUMENT TYPE: Conference; Conference Article  
TREATMENT CODE: Practical; Experimental  
COUNTRY: United States  
LANGUAGE: English  
ABSTRACT: In this article, a manufacturable material technology  
has been developed to produce highly uniform 300 mm  
**SSOI substrates**. The focus of this work has  
been on reducing defects in **SGOI** and strain  
Si layers, while maintaining high degree of  
relaxation/strain in these layers. Furthermore,  
physics of **SGOI** formation has been  
understood to the extent that key physical properties  
of the final **SGOI** layer can be accurately  
predicted based on the knowledge of the initial  
structure and subsequent processing  
CLASSIFICATION CODE: B2560R Insulated gate field effect transistors; B2550E  
Surface treatment (semiconductor technology)  
CONTROLLED TERM: elemental semiconductors; etching; Ge-  
Si alloys; **MOSFET**; silicon;  
silicon-on-insulator  
SUPPLEMENTARY TERM: manufacturable material technology; **SSOI** substrates;  
**SGOI**/strain-Si layers; relaxation degree; etching;  
**MOSFET**; **CMOS** technology; 300 mm; SiGe-Si  
CHEMICAL INDEXING: **SiGe-Si** int, **SiGe** int, Ge int, Si int, **SiGe** bin,  
Ge bin, Si bin, Si el  
PHYSICAL PROPERTIES: size 3.0E-01 m  
ELEMENT TERMS: Si; Ge\*Si; Ge sy 2; sy 2; Si sy 2; Ge-Si; SiGe; Si cp;  
cp; Ge cp; Ge

L60 ANSWER 16 OF 55 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2005:8273757 INSPEC  
DOCUMENT NUMBER: B2005-03-2560R-095  
TITLE: Fabrication and operation of sub-50 nm strained-Si on  
Sil-xGex Insulator (SGOI)  
**CMOSFETs**  
AUTHOR: Sadaka, M.; Thean, A.V.-Y.; Barr, A.; Tekleab, D.;  
Kalpat, S.; White, T.; Nguyen, T.; Mora, R.; Beckage,  
P.; Jawarani, D.; Zollner, S.; Kottke, M.; (Technol.  
Solution Organ., Freescale Semicond. Inc., Austin, TX,  
USA), Liu, R.; Canonico, M.; Xie, Q.-H.; Wang, X.-D.;  
Parsons, S.; Eades, D.; Zavala, M.; Nguyen, B.-Y.;  
Mazure, C.; Mogab, J.  
SOURCE: 2004 IEEE International SOI Conference (IEEE Cat.  
No.04CH37573), 2004, p. 209-11 of xv+216 pp., 6 refs.  
ISBN: 0 7803 8497 0  
Price: 0-7803-8497-0/04/\$20.00  
Published by: IEEE, Piscataway, NJ, USA  
Conference: 2004 IEEE International SOI Conference,  
Charleston, SC, USA, 4-7 Oct. 2004  
Sponsor(s): IEEE Electron Devices Soc  
DOCUMENT TYPE: Conference; Conference Article  
TREATMENT CODE: Practical; Experimental  
COUNTRY: United States  
LANGUAGE: English  
ABSTRACT: First functional 45 nm **SGOI CMOS**  
devices on bonded **SGOI substrates**  
with TSOI<45 nm exhibited superior short-channel  
control and comparable reliability to SOI devices. A  
67% Gm enhancement was observed in long-channel nMOS  
**SGOI devices**, 18% drive current  
increase for short-channel **SGOI devices**, and  
12% faster ring-oscillators were exhibited with  
respect to control SOI devices. Functional SRAM bit  
cells down to Vdd=0.9 V were also demonstrated  
CLASSIFICATION CODE: B2560R Insulated gate field effect transistors; B2570D  
CMOS integrated circuits; B2550N Nanometre-scale  
semiconductor fabrication technology; B1265D Memory  
circuits  
CONTROLLED TERM: **CMOS** integrated circuits; elemental  
semiconductors; **Ge-Si** alloys;  
**MOSFET**; nanotechnology; silicon-on-  
insulator; SRAM chips  
SUPPLEMENTARY TERM: sub-50 nm strained-Si layer; CMOSFET; CMOS devices;  
SGOI substrate; superior short channel control; ring  
oscillators; functional SRAM bit cell; Gm enhancement;  
drive current; strained Si on SiGe insulator; SOI  
devices; 50 nm; 45 nm; 0.9 V; SiGe-Si  
CHEMICAL INDEXING: **SiGe-Si** int, **SiGe** int, **Ge** int, **Si** int, **SiGe** bin,  
**Ge** bin, **Si** bin, **Si** el  
PHYSICAL PROPERTIES: size 5.0E-08 m; size 4.5E-08 m; voltage 9.0E-01 V  
ELEMENT TERMS: Si; Ge\*Si; Ge sy 2; sy 2; Si sy 2; SiGe; Si cp; cp; Ge  
cp; Ge-Si; Ge; Sil-xGex

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L60 ANSWER 17 OF 55 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2004:8176644 INSPEC  
DOCUMENT NUMBER: B2004-12-2570A-070  
TITLE: Stretching silicon's lifespan  
AUTHOR: Telford, M.  
SOURCE: III-Vs Review (Sept.-Oct. 2004), vol.17, no.7, p. 36-9  
CODEN: IVSRE8, ISSN: 0961-1290  
SICI: 0961-1290(200409/10)17:7L.36:SSL;1-O  
Published by: Elsevier, UK  
DOCUMENT TYPE: Journal  
TREATMENT CODE: General Review  
COUNTRY: United Kingdom  
LANGUAGE: English  
ABSTRACT: Traditional bulk silicon encounters performance limitations in shrinking **CMOS** transistor feature size to 65 nm. But, through the use of **silicon-germanium**, strained **silicon**, and **silicon-on-insulator** and, ultimately, **germanium-on-insulator** technology, the life of silicon **substrates** could be stretched as far as the 22nm generation  
CLASSIFICATION CODE: B2570A Semiconductor integrated circuit design, layout, modelling and testing; B0170E Production facilities and engineering; B2530F Metal-insulator-semiconductor structures; B2570D CMOS integrated circuits  
CONTROLLED TERM: **CMOS** integrated circuits; **Ge-Si** alloys; life testing; silicon; silicon-on-insulator  
SUPPLEMENTARY TERM: silicon lifespan; performance limitations; CMOS transistor; silicon-germanium; silicon-on-insulator technology; germanium-on-insulator technology; silicon substrates; 65 nm  
PHYSICAL PROPERTIES: size 6.5E-08 m  
ELEMENT TERMS: Si



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L60 ANSWER 23 OF 55 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2004:7933171 INSPEC  
DOCUMENT NUMBER: B2004-05-2560R-129  
TITLE: Fully depleted strained-SOI n- and p-MOSFETs  
on bonded SGOI substrates and  
study of the SiGe/BOX interface  
AUTHOR: Zhiyuan Cheng; Pitera, A.J.; Lee, M.L.; Jongwan Jung;  
Hoyt, J.L.; Antoniadis, D.A.; Fitzgerald, E.A.  
(Microsystem Technol. Labs., Massachusetts Inst. of  
Technol., Cambridge, MA, USA)  
SOURCE: IEEE Electron Device Letters (March 2004), vol.25,  
no.3, p. 147-9, 24 refs.  
CODEN: EDLEDZ, ISSN: 0741-3106  
SICI: 0741-3106(200403)25:3L:147:FDSM;1-C  
Price: 0741-3106/04/\$20.00  
Published by: IEEE, USA  
DOCUMENT TYPE: Journal  
TREATMENT CODE: Practical; Experimental  
COUNTRY: United States  
LANGUAGE: English  
ABSTRACT: Fully depleted strained-Si n- and p-MOSFETs  
have been demonstrated on bonded-SiGe-on-  
insulator (SGOI) substrates  
. The fully depleted devices show significant electron  
and hole mobility enhancements of 60 and 35%,  
respectively, demonstrating that high material  
quality, thin SGOI substrates can  
be fabricated by a wafer bonding approach. The bottom  
SiGe/buried-oxide interface in the  
SGOI structure and its impact on fully  
depleted device performance are also investigated  
CLASSIFICATION CODE: B2560R Insulated gate field effect transistors  
CONTROLLED TERM: electron mobility; elemental semiconductors;  
Ge-Si alloys; hole mobility;  
interface states; MOSFET; silicon-on-  
insulator  
SUPPLEMENTARY TERM: fully depleted strained-SOI; n-MOSFETs; p-MOSFETs;  
bonded SGOI substrates; BOX interface;  
bonded-SiGe-on-insulator; electron mobility; hole  
mobility; wafer bonding; device performance  
CHEMICAL INDEXING: SiGe int, Ge int, Si int, SiGe bin, Ge bin, Si  
bin  
ELEMENT TERMS: Si; Ge\*Si; Ge sy 2; sy 2; Si sy 2; SiGe; Si cp; cp; Ge  
cp; Ge



L60 ANSWER 26 OF 55 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2004:7820099 INSPEC  
DOCUMENT NUMBER: A2004-03-8160C-020; B2004-02-2550E-024  
TITLE: Ultrathin strained Si-on-insulator and  
SiGe-on-insulator created using low  
temperature wafer bonding and metastable stop Layers  
AUTHOR: Taraschi, G.; Pitera, A.J.; McGill, L.M.; Zhi-Yuan  
Cheng; Lee, M.L.; Langdo, T.A.; Fitzgerald, E.A.  
(Dept. of Mater. Sci. & Eng., Massachusetts Inst. of  
Technol., Cambridge, MA, USA)  
SOURCE: Journal of the Electrochemical Society (Jan. 2004),  
vol.151, no.1, p. G47-56, 36 refs.  
CODEN: JESOAN, ISSN: 0013-4651  
SICI: 0013-4651(200401)151:1L.g47:USIS;1-N  
Price: 0013-4651/2003/151(1)/G47/10/\$7.00  
Doc.No.: S0013-4651(04)02901-5  
Published by: Electrochem. Soc, USA  
DOCUMENT TYPE: Journal  
TREATMENT CODE: Practical; Experimental  
COUNTRY: United States  
LANGUAGE: English  
ABSTRACT: A method for fabricating smooth, uniform thickness,  
low defect density, monocrystalline SiGe  
alloys and strained Si on any desired  
substrate was developed, allowing for the  
creation of SiGe-on-insulator and  
strained Si-on-insulator. After wafer  
bonding and layer transfer via either delamination by  
hydrogen implantation, or back side grinding and Si  
etching, a selective SiGe etch was used to  
remove excess material and expose a strained Si stop  
layer. Recent improvements made to the process include  
more robust stop layers, low temperature wafer  
bonding, and improved selective SiGe  
etching. A major improvement involves the use of  
metastable films that allow for thicker stop layers.  
Experimental data for threading and misfit dislocation  
density for metastable Si layers on Si<sub>0.75</sub>Ge<sub>0.25</sub>  
virtual substrates is presented. Another  
improvement is the use of plasma activation prior to  
wafer bonding, allowing for strong low temperature  
bonding, while enabling metastable layers to retain  
their nonequilibrium strain state. Within the context  
of layer transfer followed by etching, a detailed  
analysis of SiGe selective etching stopping  
on strained Si was conducted. An etch consisting of  
nitric acid and dilute hydrofluoric acid was optimized  
to yield an acceptable selectively and etch rate,  
while not creating any pinholes in the exposed stop  
layer.  
CLASSIFICATION CODE: A8160C Surface treatment and degradation in  
semiconductor technology; A7340Q Electrical properties  
of metal-insulator-semiconductor structures; A6170J  
Etch pits, decoration, transmission  
electron-microscopy and other direct observations of  
dislocations; B2550E Surface treatment (semiconductor  
technology); B2530F Metal-insulator-semiconductor  
structures

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CONTROLLED TERM: delamination; dislocation density; etching; Ge  
-Si alloys; grinding; semiconductor-  
insulator boundaries; silicon-on-  
insulator; substrates; wafer bonding

SUPPLEMENTARY TERM: ultrathin strained Si-on-insulator; SiGe-on-insulator;  
low temperature wafer bonding; metastable stop layers;  
smooth uniform thickness low defect density  
monocrystalline SiGe alloys; substrate; layer  
transfer; delamination; hydrogen implantation; back  
side grinding; Si etching; selective SiGe etch;  
strained Si stop layer; selective SiGe etching; misfit  
dislocation density; threading dislocation density;  
metastable Si layers; Si<sub>0.75</sub>Ge<sub>0.25</sub> virtual substrates;  
plasma activation; nonequilibrium strain state; nitric  
acid; dilute hydrofluoric acid; pinholes; CMOS; Si;  
SiGe; Si<sub>0.75</sub>Ge<sub>0.25</sub>

CHEMICAL INDEXING: Si int, Si el; SiGe int, Ge int, Si int, SiGe  
bin, Ge bin, Si bin; Si<sub>0.75</sub>Ge<sub>0.25</sub> sur,  
Ge<sub>0.25</sub> sur, Si<sub>0.75</sub> sur, Ge sur, Si sur, Si<sub>0.75</sub>Ge<sub>0.25</sub>  
bin, Ge<sub>0.25</sub> bin, Si<sub>0.75</sub> bin, Ge bin, Si bin

ELEMENT TERMS: Si; Ge; Ge\*Si; Ge sy 2; sy 2; Si sy 2; SiGe; Si cp;  
cp; Ge cp; Si<sub>0.75</sub>Ge; Si<sub>0.75</sub>Ge<sub>0.25</sub>

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L60 ANSWER 28 OF 55 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2003:7694998 INSPEC  
DOCUMENT NUMBER: B2003-09-2560R-008  
TITLE: Ultrathin body **SiGe-on-insulator**  
pMOSFETs with high-mobility **SiGe** surface  
channels  
AUTHOR: Tezuka, T.; Sugiyama, N.; Mizuno, T.; Takagi, S. (Adv.  
LSI Technol. Lab., Toshiba Corp., Kawasaki, Japan)  
SOURCE: IEEE Transactions on Electron Devices (May 2003),  
vol.50, no.5, p. 1328-33, 21 refs.  
CODEN: IETDAI, ISSN: 0018-9383  
SICI: 0018-9383(200305)50:5L:1328:UBSI;1-A  
Price: 0018-9383/03/\$17.00  
Published by: IEEE, USA  
DOCUMENT TYPE: Journal  
TREATMENT CODE: Practical; Experimental  
COUNTRY: United States  
LANGUAGE: English  
ABSTRACT: A novel concept and a fabrication technique of  
strained **SiGe-on-insulator** (  
**SGOI**) pMOSFET are proposed and demonstrated.  
This device has an ultrathin strained **SiGe**  
channel layer, which is directly sandwiched by gate  
oxide and buried oxide layers. The mobility  
enhancement of 2.3 times higher than the universal  
mobility of conventional universal Si pMOSFETs was  
obtained for a pMOSFET with 19-nm-thick Si<sub>0.58</sub>Ge<sub>0.42</sub>  
channel layer, which is formed by high-temperature  
oxidation of a Si<sub>0.9</sub>Ge<sub>0.1</sub> layer grown on a Si-on-  
**insulator** (SOI) **substrate**. A fully  
depleted **SGOI MOSFET** with this  
simple single-layer body structure is promising for  
scaled SOI p-MOSFET with high current drive  
CLASSIFICATION CODE: B2560R Insulated gate field effect transistors; B2550E  
Surface treatment (semiconductor technology)  
CONTROLLED TERM: carrier mobility; Ge-Si alloys;  
**MOSFET**; oxidation; semiconductor materials  
SUPPLEMENTARY TERM: pMOSFETs; high-mobility SiGe surface channels; gate  
oxide; buried oxide layers; mobility enhancement;  
high-temperature oxidation; SGOI; single-layer body  
structure; current drive; 19 nm; Si<sub>0.58</sub>Ge<sub>0.42</sub>  
CHEMICAL INDEXING: Si<sub>0.58</sub>Ge<sub>0.42</sub> int, Ge<sub>0.42</sub> int, Si<sub>0.58</sub> int, Ge int,  
Si int, Si<sub>0.58</sub>Ge<sub>0.42</sub> bin, Ge<sub>0.42</sub> bin, Si<sub>0.58</sub> bin, Ge  
bin, Si bin  
PHYSICAL PROPERTIES: size 1.9E-08 m  
ELEMENT TERMS: Si; Ge\*Si; Ge sy 2; sy 2; Si sy 2; SiGe; Si cp; cp; Ge  
cp; Ge; Si<sub>0.58</sub>Ge; Si<sub>0.58</sub>Ge<sub>0.42</sub>; Si<sub>0.9</sub>Ge<sub>0.1</sub>

L60 ANSWER 31 OF 55 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2003:7671844 INSPEC  
DOCUMENT NUMBER: A2003-15-6860-014; B2003-08-2530N-002  
TITLE: Strain relaxation of strained-Si layers on  
**SiGe-on-insulator (SGOI)**  
structures after mesa isolation  
AUTHOR: Usuda, K.; Mizuno, T.; Tezuka, T.; Sugiyama, N.;  
Moriyama, Y.; Nakahari, S.; Takagi, S. (MIRAI Project,  
ASET, Kawasaki, Japan)  
SOURCE: Spatially Resolved Characterization of Local Phenomena  
in Materials and Nanostructures. Symposium (Mater.  
Res. Soc. Symposium Proceedings Vol.738), 2003, p.  
317-22 of xiii+425 pp., 9 refs.  
Editor(s): Piqueras, J.; Zypman, F.R.; Bonnell, D.A.;  
Shreve, A.P.  
ISBN: 1 55899 675 3  
Published by: Mater. Res. Soc, Warrendale, PA, USA  
Conference: Spatially Resolved Characterization of  
Local Phenomena in Materials and Nanostructures.  
Symposium, Boston, MA, USA, 2-6 Dec. 2002  
DOCUMENT TYPE: Conference; Conference Article  
TREATMENT CODE: Experimental  
COUNTRY: United States  
LANGUAGE: English  
ABSTRACT: Strained-Si-On-Insulator (Strained-SOI)  
**MOSFETs** are one of the most promising device  
structures for high speed and/or low power  
**CMOS**. In realizing strained-Si **MOS**  
LSI, fabrication of strained-Si **MOSFETs** with  
small sizes are indispensable and thus, the  
investigation of the strain relaxation is an important  
issue. Therefore, the strain relaxation of  
strained-SOI mesa islands with small active area was  
investigated in this study. Thin strained-Si films  
were grown on thin relaxed **SiGe-on-**  
**insulator (SGOI)** structures  
( $x=0.28$ ). The isolation process was carried out by  
using chemical-dry-etching (CDE) to fabricate samples  
with small active areas. Using Raman spectroscopy with  
resolution of  $>1$  micron meter, strained-Si islands on  
**SGOI substrates** with the size of 5  
micron meter square were investigated.  
Rapid-thermal-annealing (RTA) in  $N_2$  atmosphere was  
performed to study the strain relaxation during  
heating processes. As a result, it was confirmed That  
the strained-Si layers grown on relaxed SiGe ( $x=0.28$ ) before and after mesa isolation, down  
to 5 micron meter in size, had almost no relaxation  
after the RTA process at  $1000^\circ C$ . Furthermore,  
it was confirmed that the nano-beam electron  
diffraction (NBD) measurement showed similar tendency  
regarding the strain relaxation  
CLASSIFICATION CODE: A6860 Physical properties of thin films,  
nonelectronic; A6855 Thin film growth, structure, and  
epitaxy; A8160C Surface treatment and degradation in  
semiconductor technology; A7830G Infrared and Raman  
spectra in inorganic crystals; A6240 Anelasticity,  
internal friction and mechanical resonances; A6825

Mechanical and acoustical properties of solid surfaces and interfaces; A6170A Annealing processes; B2530N Other semiconductor interfaces and junctions; B2520C Elemental semiconductors; B2550E Surface treatment (semiconductor technology); B2550A Annealing processes in semiconductor technology

CONTROLLED TERM: electron diffraction; elemental semiconductors; etching; Ge-Si alloys; isolation technology; Raman spectra; rapid thermal annealing; semiconductor thin films; silicon; stress relaxation

SUPPLEMENTARY TERM: strained Si layers; SiGe on insulator structures; mesa isolation; strain relaxation; strained Si on insulator; strained SOI MOSFET device structures; low power CMOS; high speed CMOS; isolation process; chemical dry etching; Raman spectroscopy; rapid thermal annealing; RTA; N2 atmosphere; heating processes; nanobeam electron diffraction; 1000 degC; SiGe-SiO2; Si-SiGe-SiO2

CHEMICAL INDEXING: SiGeSiO2 sur, SiO2 sur, Ge sur, O2 sur, Si sur, O sur, SiGeSiO2 ss, SiO2 ss, Ge ss, O2 ss, Si ss, O ss; Si-SiGe-SiO2 int, SiGe int, SiO2 int, Ge int, O2 int, Si int, O int, SiGe bin, SiO2 bin, Ge bin, O2 bin, Si bin, O bin, Si el

PHYSICAL PROPERTIES: temperature 1.27E+03 K

ELEMENT TERMS: Si; Ge; Ge\*O\*Si; Ge sy 3; sy 3; O sy 3; Si sy 3; SiO2; Si cp; cp; O cp; Ge-SiO2; SiGe; Ge cp; SiGe-SiO2; GeSiO; O\*Si; SiO; O; SiGeSiO; SiGe-SiO; Ge\*Si; Ge sy 2; sy 2; Si sy 2; N2; C

L60 ANSWER 32 OF 55 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2003:7660105 INSPEC  
DOCUMENT NUMBER: A2003-15-7340Q-005; B2003-07-2530F-030  
TITLE: Fabrication of **SiGe-on-insulator**  
through thermal diffusion of Ge on  
**Si-on-insulator substrate**  
AUTHOR: Kutsukake, K.; Usami, N.; Fujiwara, K.; Ujihara, T.;  
Sazaki, G.; (Inst. for Mater. Res., Tohoku Univ.,  
Sendai, Japan), Zhang, B.; Segawa, Y.; Nakajima, K.  
SOURCE: Japanese Journal of Applied Physics, Part 2 (Letters)  
(1 March 2003), vol.42, no.3A, p. L232-4, 21 refs.  
CODEN: JAPLD8, ISSN: 0021-4922  
SICI: 0021-4922(20030301)42:3AL:1232:FSIT;1-X  
Published by: Japan Soc. Appl. Phys, Japan  
DOCUMENT TYPE: Journal  
TREATMENT CODE: Practical; Experimental  
COUNTRY: Japan  
LANGUAGE: English  
ABSTRACT: We report on the fabrication of a homogeneous  
**SiGe-on-insulator** as a  
**substrate** for strained **Si-on-insulator**  
(SOI) **metal-oxide-**  
**semiconductor field-effect**  
-transistors. The fabrication process includes the  
growth of a thin Ge film on a commercially available  
SOI **substrate** at 100°C using a  
molecular beam epitaxy system, the formation of a SiO<sub>2</sub>  
cap layer by radio-frequency sputtering, and rapid  
thermal annealing (RTA) in an Ar atmosphere. After RTA  
at an appropriate temperature, the **SiGe-on-**  
**insulator** with a laterally homogeneous Si  
fraction was successfully obtained by the formation of  
epitaxial **SiGe** on a thin SOI as a seed and  
interdiffusion of Ge and Si atoms.  
However, inhomogeneous **SiGe** films were  
obtained when the annealing temperature was very high.  
The conditions for the realization of **SiGe**  
with a homogeneous Si fraction were found to be  
closely related to the phase diagram of the Si  
-Ge binary alloy  
CLASSIFICATION CODE: A7340Q Electrical properties of metal-insulator-  
semiconductor structures; A6855 Thin film growth,  
structure, and epitaxy; A6170A Annealing processes;  
A6180B Ultraviolet, visible and infrared radiation  
effects; A6822 Surface diffusion, segregation and  
interfacial compound formation; B2530F  
Metal-insulator-semiconductor structures; B2560R  
Insulated gate field effect transistors; B2550A  
Annealing processes in semiconductor technology  
CONTROLLED TERM: chemical interdiffusion; **Ge-Si**  
alloys; **MOSFET**; phase diagrams; rapid  
thermal annealing; semiconductor epitaxial layers;  
semiconductor materials; semiconductor-  
**insulator** boundaries; thermal diffusion  
SUPPLEMENTARY TERM: homogeneous **SiGe-on-insulator**; SOI **MOSFETs**; thin Ge  
film; SOI substrate; molecular beam epitaxy; RF  
sputtering; rapid thermal annealing; interdiffusion;  
inhomogeneous films; phase diagram; 100 degC; **SiGe**;

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Si-SiO2  
CHEMICAL INDEXING: SiGe int, Ge int, Si int, SiGe bin, Ge bin, Si  
bin; Si-SiO2 int, SiO2 int, O2 int, Si int, O  
int, SiO2 bin, O2 bin, Si bin, O bin, Si el  
PHYSICAL PROPERTIES: temperature 3.73E+02 K  
ELEMENT TERMS: Si; Ge\*Si; Ge sy 2; sy 2; Si sy 2; SiGe; Si cp; cp; Ge  
cp; Ge; O\*Si; SiO2; O cp; SiO; O; C; Ar; Si-Ge



L60 ANSWER 35 OF 55 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2003:7493045 INSPEC  
DOCUMENT NUMBER: B2003-02-2530F-007  
TITLE: Relaxed **SiGe** on insulator  
fabricated via wafer bonding and layer transfer:  
Etch-back and smart-cut alternatives  
AUTHOR: Taraschi, G.; Zhi-Yuan Cheng; Currie, M.T.; Leitz,  
C.W.; Langdo, T.A.; Lee, M.L.; Pitera, A.; Fitzgerald,  
E.A.; (Dept. of Mater. Sci. & Eng., MIT, Cambridge,  
MA, USA), Hoyt, J.L.; Antoniadis, D.A.  
SOURCE: Silicon-on-Insulator Technology and Devices X.  
Proceedings of the Tenth International Symposium  
(Electrochemical Society Proceedings Vol.2001-3),  
2001, p. 27-32 of x+464 pp., 12 refs.  
Editor(s): Cristoloveanu, S.; Hemment, P.L.F.; Izumi,  
K.T.; Celler, G.K.; Assaderaghi, F.; Kim, Y-W  
ISBN: 1 56677 309 1  
Published by: Electrochem. Soc, Pennington, NJ, USA  
Conference: Silicon-On-Insulator Technology and  
Devices X. Proceedings of the Tenth International  
Symposium, Washington, DC, USA, 25-29 March 2001  
DOCUMENT TYPE: Conference; Conference Article  
TREATMENT CODE: Practical; Experimental  
COUNTRY: United States  
LANGUAGE: English  
ABSTRACT: **SiGe** on Insulator (**SiGeOI**) is an  
improved **substrate** for **MOS** devices  
since it combines both the benefits of an  
**insulating substrate** with those of a  
**SiGe** device layer. The fabrication process  
begins with the UHV-CVD growth of a **SiGe**  
graded layer on a **Si substrate**, followed by  
CMP to smooth the surface. For the etch-back process,  
a regrowth step is performed during which a strained  
**Si** layer etch-stop is grown followed by **Si<sub>0.75</sub>Ge<sub>0.25</sub>**.  
The **substrate** is bonded to an oxidized **Si**  
handle wafer, and the **Si** backside of the **SiGe**  
wafer is ground. Various etches are then used to  
remove the remaining **SiGe**, while stopping on  
the strained **Si**. On the other hand, for the Smart-cut  
approach, the CMPed **SiGe** wafer is  
transferred onto an oxidized **Si** handle wafer. In  
particular, the **SiGe** wafer is implanted with  
hydrogen to form a buried hydrogen-rich layer, then  
bonded and annealed to accomplish splitting at the  
hydrogen-rich region  
CLASSIFICATION CODE: B2530F Metal-insulator-semiconductor structures;  
B0520F Chemical vapour deposition; B2550E Surface  
treatment (semiconductor technology); B2520M Other  
semiconductor materials  
CONTROLLED TERM: chemical mechanical polishing; CVD coatings;  
**Ge-Si** alloys; semiconductor growth;  
semiconductor-insulator boundaries; surface  
treatment; vapour phase epitaxial growth  
SUPPLEMENTARY TERM: relaxed **SiGe** on insulator; wafer bonding; layer  
transfer; etch-back; smart-cut; **MOS** devices;  
insulating substrate; fabrication process; UHV-CVD  
growth; CMP; regrowth step; **Si<sub>0.75</sub>Ge<sub>0.25</sub>**; oxidized **Si**

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CHEMICAL INDEXING:

handle wafer; Si backside; SiGe  
SiGe int, Ge int, Si int, SiGe bin, Ge bin, Si  
bin; Si<sub>0.75</sub>Ge<sub>0.25</sub> int, Ge<sub>0.25</sub> int, Si<sub>0.75</sub>  
int, Ge int, Si int, Si<sub>0.75</sub>Ge<sub>0.25</sub> bin, Ge<sub>0.25</sub> bin,  
Si<sub>0.75</sub> bin, Ge bin, Si bin

ELEMENT TERMS:

Si; Ge\*Si; Ge sy 2; sy 2; Si sy 2; SiGe; Si cp; cp; Ge  
cp; Ge; Si<sub>0.75</sub>Ge; Ge\*I\*O\*Si; Ge sy 4; sy 4; I sy 4; O  
sy 4; Si sy 4; SiGeOI; O cp; I cp; Si<sub>0.75</sub>Ge<sub>0.25</sub>

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L60 ANSWER 36 OF 55 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2003:7491599 INSPEC  
DOCUMENT NUMBER: A2003-03-8115G-040; B2003-02-0520D-052  
TITLE: Fabrication of high-Ge fraction relaxed **SiGe**  
**-On-Insulator** virtual **substrate** by  
MBE growth and thermal annealing  
AUTHOR: Miura, A.; Irisawa, T.; Koh, S.; (Dept. of Appl.  
Phys., Univ. of Tokyo, Japan), Nakagawa, K.; Shiraki,  
Y.  
SOURCE: 2002 International Conference on Molecular Beam  
Epitaxy (Cat. No.02EX607), 2002, p. 401-2 of 424 pp.,  
2 refs.  
ISBN: 0 7803 7581 5  
Price: 0-7803-7581-5/02/\$17.00  
Published by: IEEE, Piscataway, NJ, USA  
Conference: Proceedings of MBE-XII, San Francisco, CA,  
USA, 15-20 Sept. 2002  
Sponsor(s): IEEE Lasers & Electro-Opt. Soc  
DOCUMENT TYPE: Conference; Conference Article  
TREATMENT CODE: Application; Experimental  
COUNTRY: United States  
LANGUAGE: English  
ABSTRACT: **SiGe-On-Insulator (SGOI)**  
is a promising structure that allows the fabrication  
of high speed, low power consumption sub-100 nm  
complementary-metal-oxide-  
**semiconductor (CMOS)**. Much research  
has been previously made on **SGOI** virtual  
**substrates** with the Ge concentration of 10%  
30%, which is used for strained-Si channel  
**metal-oxide-semiconductor**  
**field-effect-transistors (**  
**MOSFETs)**. However, no reports have been ever  
made on strained-Ge channel structures grown on  
**SGOI** virtual **substrates**, though  
strained-Ge channel devices demonstrate very high  
mobilities, which indicates that the combination of  
these structures with the **SGOI** technology is  
promising. In order to grow strained-Ge channels on  
**SGOI** virtual **substrates**, a high Ge  
fraction of 60% 70% is necessary. We report on the  
first attempt of the fabrication of high-Ge fraction  
relaxed **SGOI** virtual **substrate** by  
MBE growth and thermal diffusion. We have achieved a  
single crystal high-Ge fraction ( 64%) layer, a smooth  
surface ( 0.4 nm rms), complete strain relaxation, and  
an almost uniform Ge distribution  
CLASSIFICATION CODE: A8115G Vacuum deposition; A6855 Thin film growth,  
structure, and epitaxy; A6170A Annealing processes;  
A6860 Physical properties of thin films,  
nonelectronic; B0520D Vacuum deposition; B2550A  
Annealing processes in semiconductor technology;  
B2520M Other semiconductor materials  
CONTROLLED TERM: annealing; atomic force microscopy; Ge-  
Si alloys; molecular beam epitaxial growth;  
Rutherford backscattering; semiconductor growth;  
semiconductor materials; stress relaxation;  
**substrates**; thermal diffusion; X-ray

EIC 2800 MARY S. MIMS 272-5928

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SUPPLEMENTARY TERM: diffraction  
fabrication; high-Ge fraction relaxed  
SiGe-On-Insulator virtual substrate; MBE growth;  
thermal annealing; SGOI; low power consumption; CMOS;  
Ge concentration; MOSFETs; strained-Ge channel  
structures; thermal diffusion; single crystal high-Ge  
fraction layer; smooth surface; strain relaxation;  
almost uniform Ge distribution; atomic force  
microscopy; X-ray diffraction; Rutherford  
backscattering; SiGe

CHEMICAL INDEXING: SiGe sur, Ge sur, Si sur, SiGe bin, Ge bin, Si  
bin; SiGe int, Ge int, Si int, SiGe bin, Ge  
bin, Si bin

ELEMENT TERMS: Si; Ge; Ge sy 2; sy 2; Si sy 2; SiGe; Si cp; cp; Ge  
cp; Ge\*Si

02/06/2007 10/710826 Doty

L60 ANSWER 53 OF 55 INSPEC (C) 2007 IET on STN

ACCESSION NUMBER: 2001:6867455 INSPEC

DOCUMENT NUMBER: B2001-04-2560S-029

TITLE: **SiGe-on-insulator** prepared by wafer bonding and layer transfer for high-performance **field-effect** transistors

AUTHOR: Huang, L.J.; Chu, J.O.; Canaperi, D.F.; D'Emic, C.P.; Anderson, R.M.; Koester, S.J.; Wong, H.-S.P. (IBM T.J. Watson Res. Center, Yorktown Heights, NY, USA)

SOURCE: Applied Physics Letters (26 Feb. 2001), vol.78, no.9, p. 1267-9, 12 refs.

CODEN: APPLAB, ISSN: 0003-6951

SICI: 0003-6951(20010226)78:9L:1267:SIPW;1-0

Price: 0003-6951/2001/78(9)/1267(3)/\$18.00

Doc.No.: S0003-6951(01)05204-4

Published by: AIP, USA

DOCUMENT TYPE: Journal

TREATMENT CODE: Practical; Experimental

COUNTRY: United States

LANGUAGE: English

ABSTRACT: **SiGe-on-insulator** material was fabricated by wafer bonding and hydrogen-induced layer transfer techniques. The transferred **SiGe** layer is strain relaxed and has a Ge content ranging from 15% to 25%. High-quality strained Si layers were grown on the **SiGe-on-insulator substrates** by the UHV/chemical vapor deposition process at 550°C. An electron mobility of 40 000 cm<sup>2</sup>/V s in a modulation-doped Si/**SiGe** heterostructure was achieved at 30 K on a **SiGe-on-insulator substrate**

CLASSIFICATION CODE: B2560S Other field effect devices; B0520F Chemical vapour deposition

CONTROLLED TERM: chemical vapour deposition; electron mobility; elemental semiconductors; **Ge-Si** alloys; high electron mobility transistors; internal stresses; semiconductor device measurement; semiconductor growth; semiconductor materials; semiconductor-**insulator** boundaries; silicon; stoichiometry; stress relaxation; wafer bonding

SUPPLEMENTARY TERM: **SiGe-on-insulator**; wafer bonding; layer transfer; high-performance field-effect transistors; hydrogen-induced layer transfer techniques; Ge content; high-quality strained Si layers; UHV/chemical vapor deposition process; electron mobility; modulation-doped Si/**SiGe** heterostructure;

CHEMICAL INDEXING: **SiGe-on-insulator** substrate; 30 K; 550 C; Si-GeSi **Si-GeSi** int, **GeSi** int, **Ge** int, **Si** int, **GeSi** bin, **Ge** bin, **Si** bin, **Si** el

PHYSICAL PROPERTIES: temperature 3.0E+01 K; temperature 8.23E+02 K

ELEMENT TERMS: Si; Ge; Ge\*Si; Ge sy 2; sy 2; Si sy 2; **SiGe**; Si cp; cp; Ge cp; **GeSi**; C

02/06/2007 10/710826 Doty

L60 ANSWER 4 OF 55 INSPEC (C) 2007 IET on STN  
ACCESSION NUMBER: 2006:8870673 INSPEC  
TITLE: Hole mobility enhancement in strained-Si/strained-SiGe heterostructure p-MOSFETs fabricated on SiGe-on-insulator (SGOI)  
AUTHOR: Zhiyuan Cheng; Jongwan Jung; Minjoo L Lee; Pitera, A.J.; Hoyt, J.L.; Antoniadis, D.A.; Fitzgerald, E.A. (Microsyst. Technol. Lab., MIT, Cambridge, MA, USA)  
SOURCE: Semiconductor Science and Technology (May 2004), vol.19, no.5, p. L48-51, 26 refs.  
CODEN: SSTEET, ISSN: 0268-1242  
SICI: 0268-1242(200405)19:5L:148:HMES;1-O  
Price: 0268-1242/04/050048+04\$30.00  
Doc.No.: S0268-1242(04)72643-7  
Published by: IOP Publishing, UK  
DOCUMENT TYPE: Journal  
TREATMENT CODE: Experimental  
COUNTRY: United Kingdom  
LANGUAGE: English  
ABSTRACT: Dual-channel heterostructures, with a tensile strained-Si layer (for electron channel) and a compressively strained-Si<sub>0.4</sub>Ge<sub>0.6</sub> layer (for hole channel) on relaxed-Si<sub>0.7</sub>Ge<sub>0.3</sub>-on-insulator (SGOI) substrates were fabricated by bond, etch-back and epitaxial regrowth. Partially depleted p-MOSFETs were made on this strained-Si/strained-SiGe SGOI heterostructure. The hole mobility shows an enhancement of about 1.8 times at 0.2 MV cm<sup>-1</sup>, equivalent to that obtained on co-processed strained-Si/strained-SiGe p-MOSFETs fabricated on bulk relaxed Si<sub>0.7</sub>Ge<sub>0.3</sub> virtual substrates. The limited thermal budget issue for this heterostructure is also discussed  
CLASSIFICATION CODE: B2560R Insulated gate field effect transistors; B2530F Metal-insulator-semiconductor structures  
CONTROLLED TERM: Ge-Si alloys; hole mobility; MOSFET; semiconductor heterojunctions; semiconductor-insulator boundaries  
SUPPLEMENTARY TERM: dual-channel heterostructure p-MOSFETs; SiGe-On-Insulator; tensile strained-Si channel; compressively strained-Si<sub>0.4</sub>Ge<sub>0.6</sub> channel; relaxed-Si<sub>0.7</sub>Ge<sub>0.3</sub>-on-insulator; bond; etch-back; epitaxial regrowth; hole mobility; partially-depleted p-MOSFET's; limited thermal budget; Si<sub>0.4</sub>Ge<sub>0.6</sub>; Si<sub>0.7</sub>Ge<sub>0.3</sub>; Si  
CHEMICAL INDEXING: Si<sub>0.4</sub>Ge<sub>0.6</sub> int, Ge<sub>0.6</sub> int, Si<sub>0.4</sub> int, Ge int, Si int, Si<sub>0.4</sub>Ge<sub>0.6</sub> bin, Ge<sub>0.6</sub> bin, Si<sub>0.4</sub> bin, Ge bin, Si bin; Si<sub>0.7</sub>Ge<sub>0.3</sub> int, Ge<sub>0.3</sub> int, Si<sub>0.7</sub> int, Ge int, Si int, Si<sub>0.7</sub>Ge<sub>0.3</sub> bin, Ge<sub>0.3</sub> bin, Si<sub>0.7</sub> bin, Ge bin, Si bin; Si int, Si el  
ELEMENT TERMS: Ge\*Si; Ge sy 2; sy 2; Si sy 2; Ge-Si; Ge; Si; Si<sub>0.4</sub>Ge<sub>0.6</sub>; Si cp; cp; Ge cp; Si<sub>0.7</sub>Ge<sub>0.3</sub>; Si<sub>0.4</sub>Ge; Si<sub>0.7</sub>Ge; SiGe

02/06/2007 10/710826 Doty

L36 ANSWER 12 OF 20 JAPIO (C) 2007 JPO on STN

ACCESSION NUMBER: 2006-019725 JAPIO

TITLE: STRAINED SiMOSEFT ON TENSILE STRAIN SiGe-ON-  
INSULATOR (SGOI)

INVENTOR: KEVIN K CHAN; CHU JACK O; KERN LIM; SHI LEATHEN

PATENT ASSIGNEE(S): INTERNATL BUSINESS MACH CORP <IBM>

PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 2006019725	A	20060119	Heisei	

APPLICATION INFORMATION

STN FORMAT: JP 2005-182416 20050622

ORIGINAL: JP2005182416 Heisei

PRIORITY APPLN. INFO.: US 2004-883443 20040701

SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined  
Applications, Vol. 2006

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a formation method for a heterostructure that can separate the fact that high strain is preferred in a strain Si layer and a Ge content in a low layer.

SOLUTION: A first multilayered structure 10 of a strained Si layer 14 and tensile strain SiGe alloy layer 16 constitute on a relaxation SiGe alloy layer 12. Then, a second multilayered structure 18, including an insulating layer 20, is formed on a substrate 22 and jointed with the first multilayered structure 10. After the insulating layer 20 and the SiGe alloy layer 16 are jointed, the relaxing SiGe alloy layer 12 is completely removed.

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02/06/2007 10/710826 Doty

L28 ANSWER 3 OF 6 WPIX COPYRIGHT 2007 THE THOMSON CORP on STN  
ACCESSION NUMBER: 2005-260662 [27] WPIX  
DOC. NO. CPI: C2005-082381 [27]  
DOC. NO. NON-CPI: N2005-213974 [27]  
TITLE: Fabricating silicon germanide-on-insulator substrate material used in e.g. lattice mismatched structures, by annealing silicon-containing substrate and germanium-containing layer including a porous region beneath germanium-containing layer  
DERWENT CLASS: L03; U11  
INVENTOR: BEDELL S W; CHOE K S; FOGEL K E; FOGEL K F; SADANA D K; BEDELL S; FOGEL K; SADANA D  
PATENT ASSIGNEE: (IBMC-C) INT BUSINESS MACHINES CORP  
COUNTRY COUNT: 107

PATENT INFORMATION:

PATENT NO	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 20050056352	A1	20050317	(200527)*	EN	15[6]	
WO 2005031810	A2	20050407	(200527)	EN		
EP 1665340	A2	20060607	(200638)	EN		H01L021-00
US 7125458	B2	20061024	(200670)	EN		
KR 2006061839	A	20060608	(200674)	KO		

PRIORITY APPLN. INFO: US 2003-662028 20030912

INT. PATENT CLASSIF.:

IPC ORIGINAL: H01L0021-00 [I,A]; H01L0021-02 [I,C]; H01L0021-20 [I,A]; H01L0027-12 [I,A]

IPC RECLASSIF.: H01L0021-02 [I,C]; H01L0021-20 [I,A]; H01L0021-70 [I,C]; H01L0021-762 [I,A]

BASIC ABSTRACT:

US 20050056352 A1 UPAB: 20051221

NOVELTY - A silicon germanide-on-insulator substrate material is fabricated by: providing a structure comprising a silicon-containing substrate (10) having a hole-rich region and a germanium-containing layer (14) atop the silicon-containing substrate; converting the one hole-rich region into a porous region (16); and annealing the structure including the porous region to provide a relaxed **silicon germanium-on-insulator** material.

USE - The method is used for fabricating **SiGe-on-insulator** substrate material used as lattice mismatched template, i.e. substrate, for forming strained Si layers. It is used in **superlattice** structures and lattice mismatched structures. It is useful in high-performance complementary metal oxide semiconductor (CMOS) applications.

ADVANTAGE - The method does not employ wafer bonding and/or oxygen implantation in the fabrication process. It can fabricate a thin, high-quality relaxed **SiGe-on-insulator** that is thermodynamically stable against defect production such as misfit and threading dislocations and that is compatible with CMOS processing steps.

DESCRIPTION OF DRAWINGS - The figure is a pictorial view showing the basic processing step in fabricating **SiGe-on-insulator** substrate material.

Silicon-containing substrate (10)  
Germanium-containing layer (14)  
Porous region (16)

TECHNOLOGY FOCUS:

INORGANIC CHEMISTRY - Preferred Method: The providing step comprises growing a p-rich epitaxial layer on an initial silicon(Si)-containing substrate, forming a single crystal Si-containing layer atop the p-rich epitaxial layer, and forming the germanium(Ge)-containing layer on the single crystal Si-containing layer; ion implanting a p-type dopant into an initial single crystal Si-containing substrate and then forming the Ge-containing layer on the substrate; or forming the Ge-containing layer on an initial single crystal Si-containing substrate and then implanting p-type dopant into the substrate to form the hole-rich region.

The boron is implanted at an energy of 100-500 keV and a dose of  $5E15$ - $5E16$  atom/cm<sup>2</sup>.

The boron difluoride is implanted at an energy of 500-2500 keV and a dose of  $5E15$ - $5E16$  atom/cm<sup>2</sup>.

The method further comprises an annealing step, such as furnace anneal, rapid thermal anneal, or spike anneal.

The furnace anneal step is carried out at greater than or equal to 600 degrees C for greater than or equal to 15 minutes in the presence of an inert gas atmosphere and/or an oxidizing ambient.

The rapid thermal anneal step is carried out at greater than or equal to 800 degrees C for less than or equal to 5 minutes in the presence of an inert gas atmosphere and/or an oxidizing ambient.

The spike annealing step is performed at greater than or equal to 900 degrees C for less than or equal to 1 second in the presence of an inert gas atmosphere and/or an oxidizing ambient.

The converting step comprises an electrolytic anodization process, which is performed in the presence of hydrofluoric acid-containing solution and using a constant current source operating at a current density of 0.05-50 milliAmps/cm<sup>2</sup>.

The method further comprises forming a cap layer atop the Ge-containing layer after the converting step, but before the annealing step. The annealing step forms a surface oxide atop the relaxed **SiGe-on-insulator** material.

Preferred Components: The p-type dopant is gallium, aluminum, boron or boron difluoride. The hole-rich region has a p-type dopant concentration of greater than or equal to  $1E19$  or  $1E20$ - $5E20$  atoms/cm<sup>3</sup>. The oxygen-containing ambient further comprises an inert gas. It consists of oxygen (O<sub>2</sub>), nitric oxide (NO), nitrous oxide (N<sub>2</sub>O), ozone, or air. The insulator of the **SiGe-on-insulator** material is a thermal oxide. The cap layer comprises a Si material. The porous region has a porosity of greater than or equal to 1%.

ORGANIC CHEMISTRY - Preferred Method: The providing step comprises growing a p-rich epitaxial layer on an initial silicon(Si)-containing substrate, forming a single crystal Si-containing layer atop the p-rich epitaxial layer, and forming the germanium(Ge)-containing layer on the single crystal Si-containing layer; ion implanting a p-type dopant into an initial single crystal Si-containing substrate and then forming the Ge-containing layer on the substrate; or forming the Ge-containing layer on an initial single crystal Si-containing substrate and then implanting p-type dopant into the substrate to form the hole-rich region.

The boron is implanted at an energy of 100-500 keV and a dose of  $5E15$ - $5E16$  atom/cm<sup>2</sup>.

The boron difluoride is implanted at an energy of 500-2500 keV and a dose of  $5E15$ - $5E16$  atom/cm<sup>2</sup>.

The method further comprises an annealing step, such as furnace anneal, rapid thermal anneal, or spike anneal.

The furnace anneal step is carried out at greater than or equal to 600 degrees C for greater than or equal to 15 minutes in the presence of

an inert gas atmosphere and/or an oxidizing ambient.

The rapid thermal anneal step is carried out at greater than or equal to 800 degrees C for less than or equal to 5 minutes in the presence of an inert gas atmosphere and/or an oxidizing ambient.

The spike annealing step is performed at greater than or equal to 900 degrees C for less than or equal to 1 second in the presence of an inert gas atmosphere and/or an oxidizing ambient.

The converting step comprises an electrolytic anodization process, which is performed in the presence of hydrofluoric acid-containing solution and using a constant current source operating at a current density of 0.05-50 milliAmps/cm<sup>2</sup>.

The method further comprises forming a cap layer atop the Ge-containing layer after the converting step, but before the annealing step. The annealing step forms a surface oxide atop the relaxed **SiGe-on-insulator** material.

Preferred Components: The p-type dopant is gallium, aluminum, boron or boron difluoride. The hole-rich region has a p-type dopant concentration of greater than or equal to 1E19 or 1E20-5E20 atoms/cm<sup>3</sup>. The oxygen-containing ambient further comprises an inert gas. It consists of oxygen (O<sub>2</sub>), nitric oxide (NO), nitrous oxide (N<sub>2</sub>O), ozone, or air. The insulator of the **SiGe-on-insulator** material is a thermal oxide. The cap layer comprises a Si material. The porous region has a porosity of greater than or equal to 1%.

FILE SEGMENT: CPI; EPI  
MANUAL CODE: CPI: L04-C02B; L04-C16A; L04-C22  
EPI: U11-C08A6

02/06/2007 10/710826 Doty

L36 ANSWER 20 OF 20 JAPIO (C) 2007 JPO on STN  
ACCESSION NUMBER: 2004-040122 JAPIO  
TITLE: **SiGe-ON-INSULATOR** SUBSTRATE  
MATERIAL AND METHOD FOR FABRICATING THE SAME  
INVENTOR: BEDELL STEPHEN W; FOGEL KEITH E; DEVENDORA K SADANA  
PATENT ASSIGNEE(S): INTERNATL BUSINESS MACH CORP <IBM>  
PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 2004040122	A	20040205	Heisei	H01L021-20

APPLICATION INFORMATION

STN FORMAT: JP 2003-274987 20030715  
ORIGINAL: JP2003274987 Heisei  
PRIORITY APPLN. INFO.: US 2002-196611 20020716  
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined  
Applications, Vol. 2004

INT. PATENT CLASSIF.:

MAIN: H01L021-20  
SECONDARY: H01L021-265; H01L029-161

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a method for forming a relaxed **SiGe-on-insulator** substrate having improved relaxation, comparatively low defect density, and improved surface quality.  
SOLUTION: The method includes a step for forming a **SiGe** alloy layer on a surface of a first single crystal Si layer. The first single crystal Si layer has an interface with an underlay barrier layer having resistance to Ge diffusion. Next, ions are implanted into the structure, the ions forming defects by which mechanical decoupling is achieved at the interface or vicinity of the interface; then a heating step is performed to the structure including the implanted ions, by which mutual diffusion of Ge through the first single crystal Si layer and **SiGe** layer is achieved; thereby a **SiGe** layer that is substantially relaxed single crystal and homogenous is formed on the barrier layer. A **SiGe-on-insulator** having improved properties and a heterostructure including it are also provided.  
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L24 ANSWER 5 OF 5 CAPLUS COPYRIGHT 2007 ACS on STN

ACCESSION NUMBER: 2003:594885 CAPLUS

DOCUMENT NUMBER: 139:268590

TITLE: Hole mobility enhancements in nanometer-scale strained-silicon heterostructures grown on Ge-rich relaxed Si<sub>1-x</sub>Ge<sub>x</sub>

AUTHOR(S): Lee, Minjoo L.; Fitzgerald, Eugene A.

CORPORATE SOURCE: Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, MA, 02139, USA

SOURCE: Journal of Applied Physics (2003), 94(4), 2590-2596

CODEN: JAPIAU; ISSN: 0021-8979

PUBLISHER: American Institute of Physics

DOCUMENT TYPE: Journal

LANGUAGE: English

AB Although strained-silicon ( $\epsilon$ -Si) p-type metal-oxide-semiconductor field-effect transistors (p-MOSFETs) demonstrate enhanced hole mobility compared to bulk Si devices, the enhancement has widely been observed to degrade at large vertical effective fields. The authors conjecture that the hole wave function in  $\epsilon$ -Si heterostructures spreads out over distances of  $\sim 10$  nm, even at large inversion densities, due to the strain-induced reduction of the out-of-plane effective mass. Relevant exptl. and theor. studies supporting this argument are presented. The authors further hypothesize that by growing layers thinner than the hole wave function itself, inversion carriers can be forced to occupy and hybridize the valence bands of different materials. In this article, they show that p-MOSFETs with thin (i.e.,  $< 3$  nm)  $\epsilon$ -Si layers grown on Ge-rich Si<sub>1-x</sub>Ge<sub>x</sub> buffers exhibit markedly different mobility enhancements from prior  $\epsilon$ -Si p-MOSFETs. Devices fabricated on a thin  $\epsilon$ -Si layer grown on relaxed Si<sub>0.3</sub>Ge<sub>0.7</sub> demonstrate hole mobility enhancements that increase with gate overdrive, peaking at a value of nearly 3 times. In other devices where the channel region consists of a periodic  $\epsilon$ -Si/relaxed Si<sub>0.3</sub>Ge<sub>0.7</sub> **digital alloy**, a nearly constant mobility enhancement of 2.0 was observed over inversion densities ranging from  $3 \times 10^{12}$  to  $14 \times 10^{12}$  cm<sup>-2</sup>.

IT 12675-06-8, Germanium 60, silicon 40 (atomic)

83573-93-7, Germanium 70, silicon 30 (atomic)

RL: TEM (Technical or engineered material use); USES (Uses)  
(hole mobility enhancements in nm-scale strained-silicon heterostructures grown on Ge-rich relaxed Si<sub>1-x</sub>Ge<sub>x</sub>)

RN 12675-06-8 CAPLUS

CN Germanium alloy, base, Ge 79, Si 21 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Ge	79	7440-56-4
Si	21	7440-21-3

RN 83573-93-7 CAPLUS

CN Germanium alloy, base, Ge 86, Si 14 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Ge	86	7440-56-4
Si	14	7440-21-3

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02/06/2007 10/710826 Doty

CC 76-3 (Electric Phenomena)

ST hole mobility **silicon germanium** heterostructure

IT 7440-21-3, Silicon, uses 12675-06-8, **Germanium** 60,

**silicon** 40 (atomic) 83573-93-7, **Germanium** 70,

**silicon** 30 (atomic)

RL: TEM (Technical or engineered material use); USES (Uses)

(hole mobility enhancements in nm-scale strained-silicon

heterostructures grown on Ge-rich relaxed Si<sub>1-x</sub>Gex)

REFERENCE COUNT: . 29 THERE ARE 29 CITED REFERENCES AVAILABLE FOR THIS  
RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT



02/06/2007 10/710826 Doty

L10 ANSWER 2 OF 13 CAPLUS COPYRIGHT 2007 ACS on STN

ACCESSION NUMBER: 2006:84196 CAPLUS

DOCUMENT NUMBER: 144:201536

TITLE: Raman amplification and lasing in SiGe-on-insulator waveguides

AUTHOR(S): Raghunathan, V.; Claps, R.; Boyraz, O.; Koonath, P.; Dimitropoulos, D.; Jalali, B.

CORPORATE SOURCE: Optoelectronic Circuits and Systems Laboratory, University of California, Los Angeles, USA

SOURCE: Proceedings - IEEE International SOI Conference, Honolulu, HI, United States, Oct. 3-6, 2005 (2005), 196-197. Institute of Electrical and Electronics Engineers: New York, N. Y.

CODEN: 69HTM5; ISBN: 0-7803-9212-4

DOCUMENT TYPE: Conference

LANGUAGE: English

AB Layers of Si<sub>1-x</sub>Ge<sub>x</sub> were grown on SOI substrates by CVD under non-equilibrium conditions, and pulsed-pump measurements of the stimulated Raman amplification were performed. The obtained results for the SiGe SOI waveguide were compared with those for a pure Si SOI waveguide. The effect of the SiGe **superlattice** on the Raman spectra is discussed. The theor. shift (-2.7 cm<sup>-1</sup> or 70 GHz) is 50% larger than the exptl. observed one. This was explained by the fact that not all of the optical modes were confined within the SiGe layer. The SiGe layer on the SOI platform represents a Raman medium with a flexible gain spectrum.

IT 11148-21-3

RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PRP (Properties); PYP (Physical process); PROC (Process); USES (Uses)

(Raman amplification and lasing in SiGe-on-**insulator** waveguides)

RN 11148-21-3 CAPLUS

CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component Component  
Registry Number

=====+=====

Ge 7440-56-4

Si 7440-21-3

CC 73-10 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)

Section cross-reference(s): 76

IT 11148-21-3

RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PRP (Properties); PYP (Physical process); PROC (Process); USES (Uses)

(Raman amplification and lasing in SiGe-on-**insulator** waveguides)

REFERENCE COUNT: 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT